Research Scholars Forum
Department of Electronics and Electrical Engineering

One Day Workshop on MEMS

An initiative of Research Scholars Forum,
Department of Electronics and Electrical Engineering,
Indian Institute of Technology Guwahati

In Collaboration with
IEEE-EDS Student Branch Chapter
NIT Silchar,

Research
Scholars
Outreach

Research Scholars Forum
Electronics and Electrical Engineering
Indian Institute of Technology Guwahati

Introduction to MEMS

- What is MEMS?
- What do MEMS devices look like?
- What can they do?

What are MEMS?

Acronym for micro-electro-mechanical systems.

Micro: Small size. The basic unit of measure is the micrometer or micron (μm)

$$1\ \mu m = 10^{-6}\ m$$

Electro: MEMS have electrical components

Mechanical: MEMS have moving parts

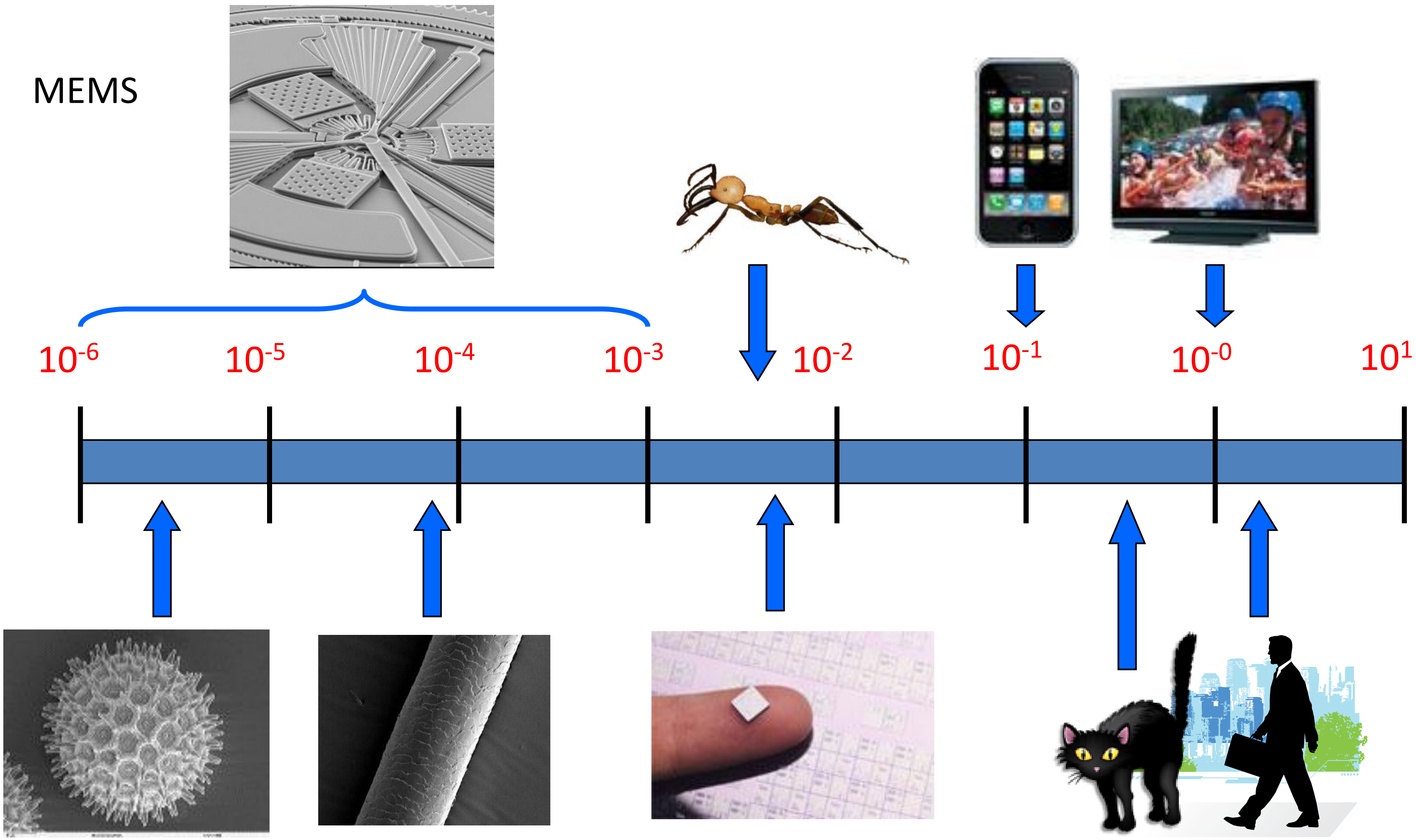
Systems: Refers to integration of components.

Examples of MEMS

You can find MEMS in

- Automobiles (Air bag sensors)
- Computer printers (Ink jet print heads)
- Cell phones (RF devices)
- Lab-on-a-chip (Microfluidics)
- Optical devices (Micromirrors)
- Lots of other things

Scales and Dimensions - MEMS



Pollen

Human hair
(ϕ 80-100μm)

Silicon die
(5 x 5 mm)

Why go micro?

What are some reasons that you would want to make micro-sized devices?

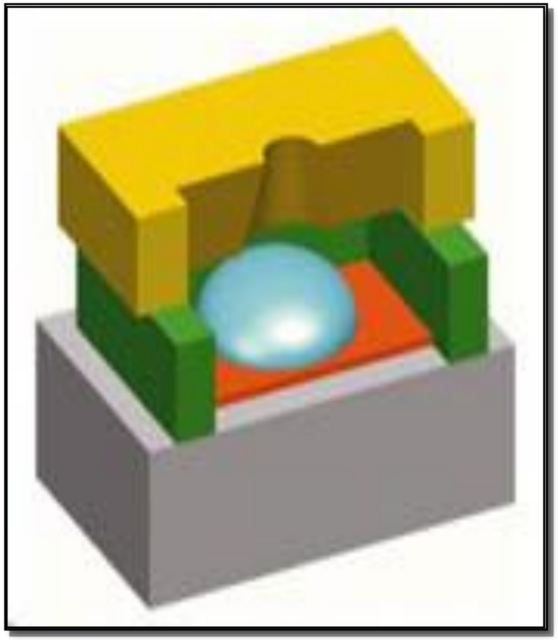
- Smaller devices require less material to make. (Earth has limited resources.)
- Smaller devices require less energy to run.
- Redundancy can lead to increased safety. (You can use an array of sensors instead of just one.)
- Micro devices are inexpensive (?)
  - Less material
  - Can be fabricated in **batch processes**

Ink jet print heads

Ink dots are tiny (10-30 per mm) and so are the nozzles that fire them.

Ink jet print heads

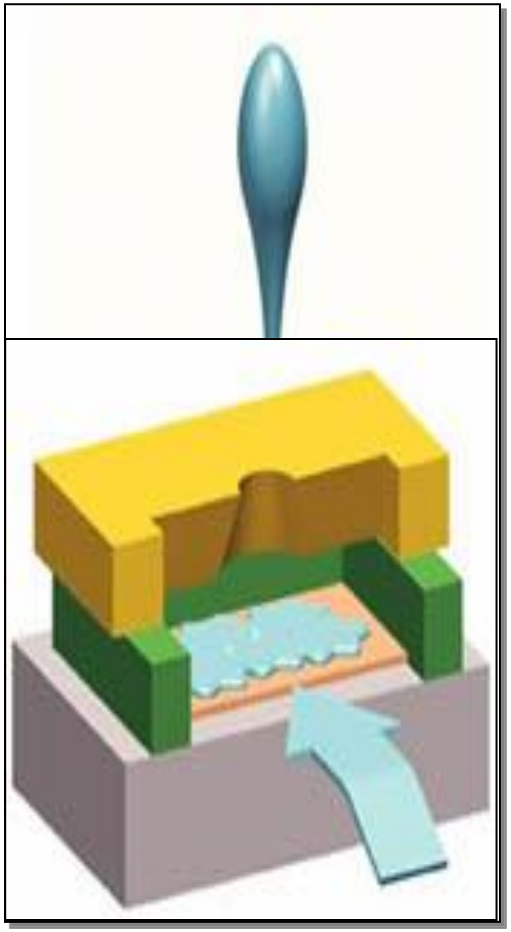
- Ink-filled chambers are heated by tiny resistive heating element
- By heating the liquid ink a bubble is generated



Ink jet print heads

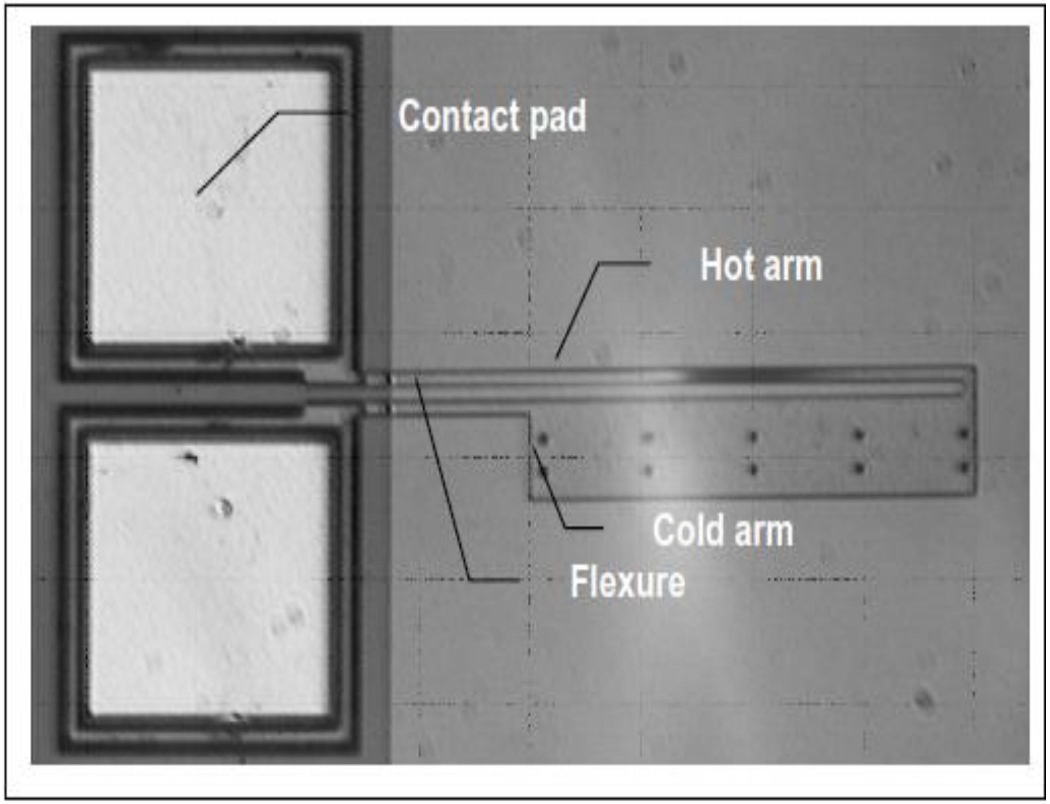
- The vaporized part of the ink is propelled towards the paper in a tiny droplet

- Chambers are filled again by the ink through microscopic channels



Examples of small scale effects

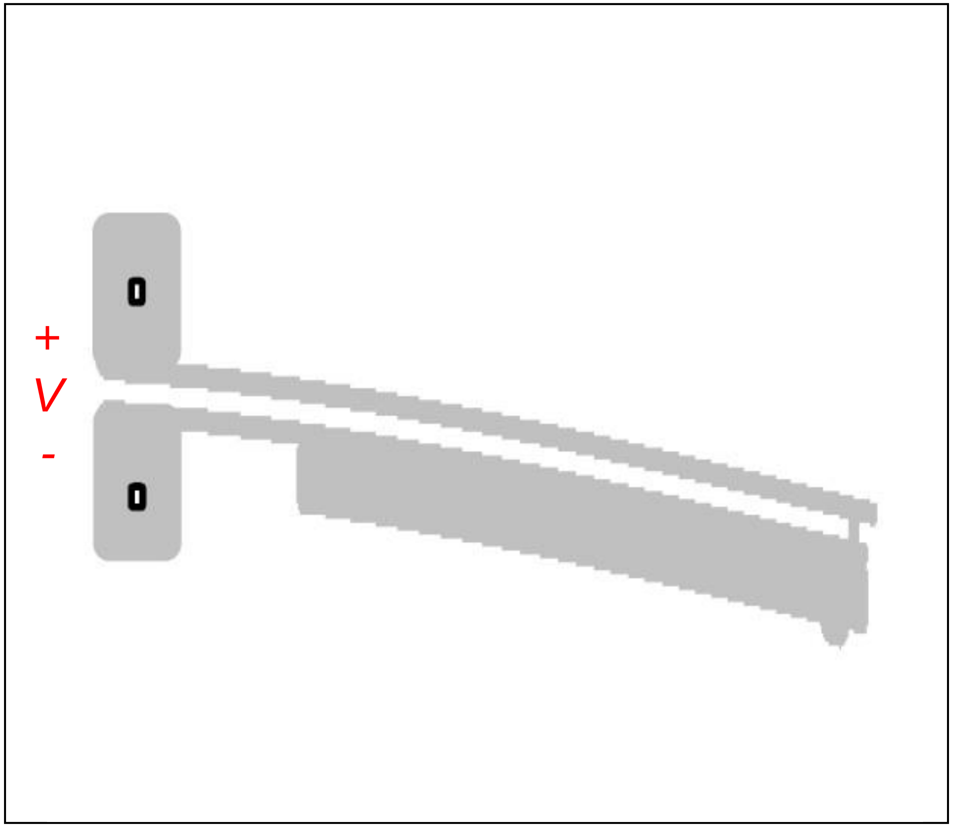
Hot arm actuator



A poly-silicon hot-arm actuator fabricated using surface micromachining

Examples of small scale effects

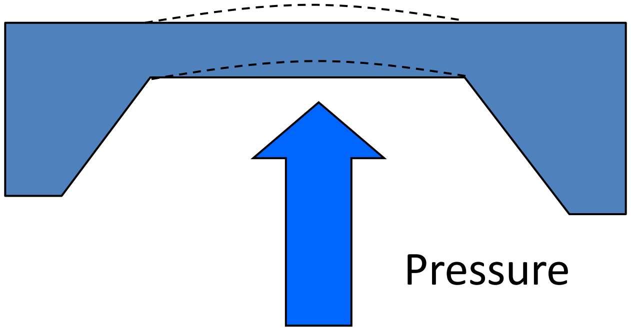
Hot arm actuator



A poly-silicon hot-arm actuator fabricated using surface micromachining

Examples- Pressure Sensors

Pressure sensors utilise an thin membrane formed on or in the silicon chip.



Sensing mechanism detects the movement of the diaphragm. Signal conditioning electronics integrated on the same die.

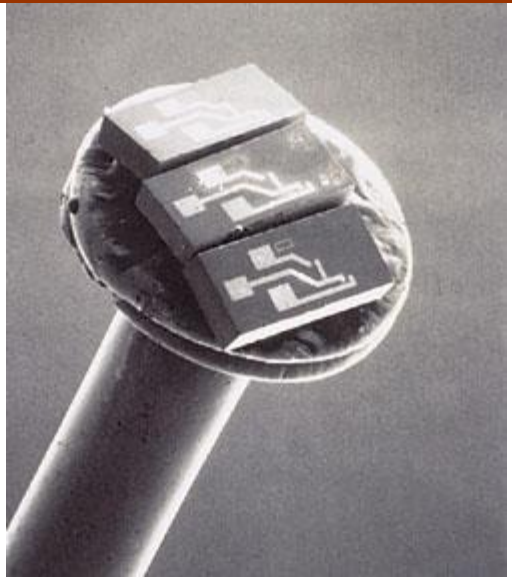
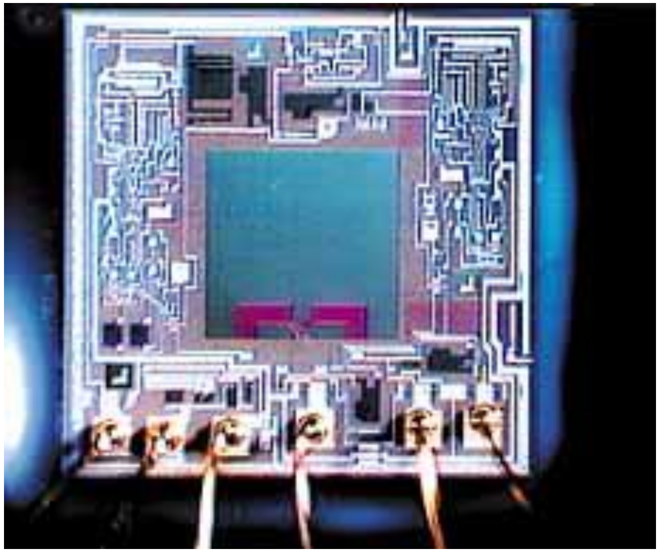


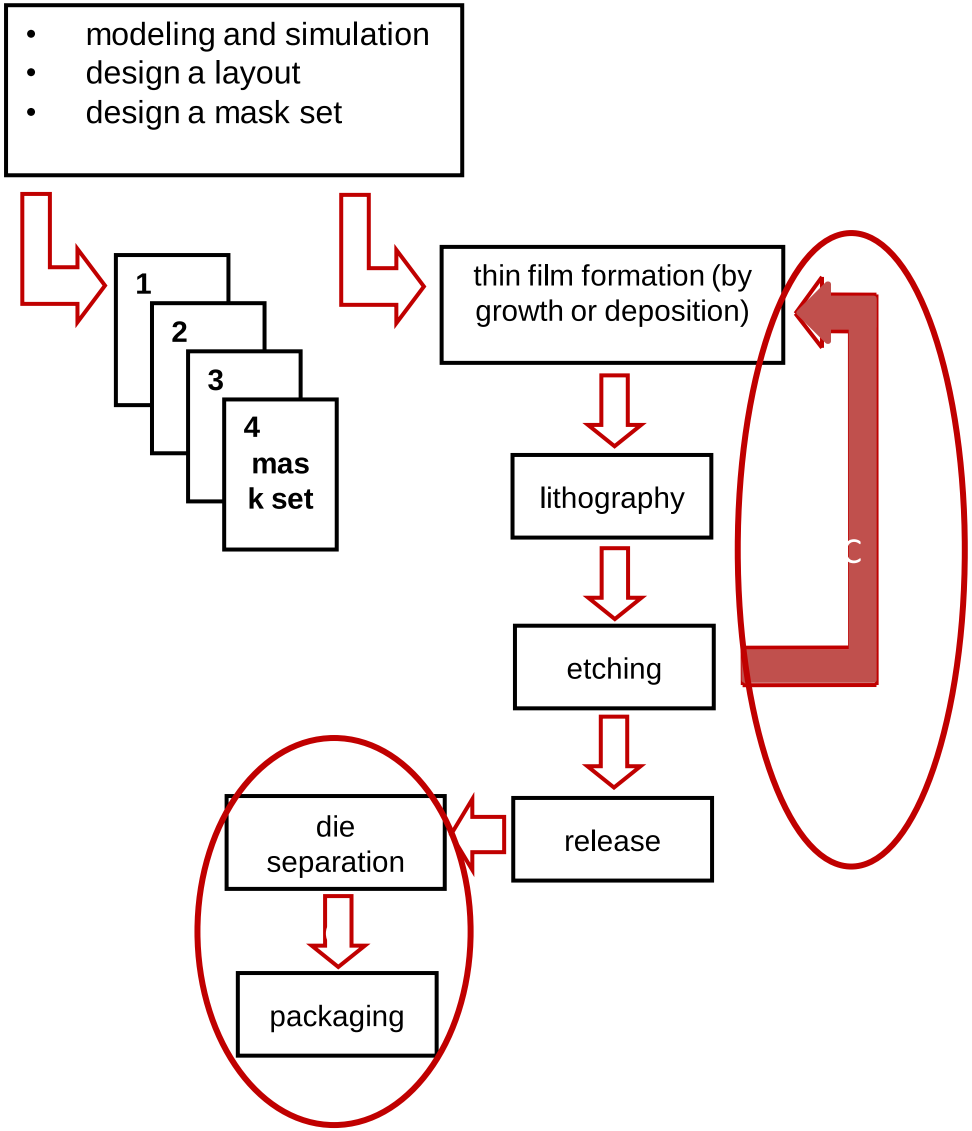
Photo from GE Novasensor – Catheter pressure sensors



Factors to Consider

- MEMS requires a mechanical structure specifically designed for the application
- The fabrication process must be considered at the outset since this defines dimensional limits and material properties
- Most MEMS use silicon but plastics, ceramics and glasses can be used

Typical process steps



- modeling and simulation
- design a layout
- design a mask set

1

2

3

4 mas k set

thin film formation (by growth or deposition)

lithography

etching

release

die separation

packaging

This is where process flow becomes complicated.

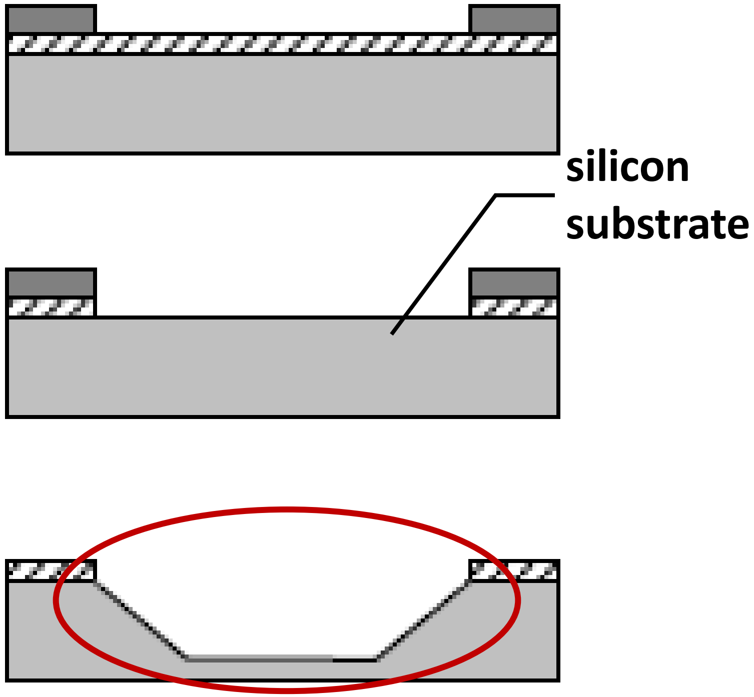
Some Useful Resources

- Periodicals
  - IEEE/ASME, JMEMS
  - Sensors and Actuators A/B
  - J. Micromechanics and Microengineering
  - Sensors and Materials
- Articles
  - Petersen, *Silicon as a Mechanical Material*, Proc. IEEE, V70 pp.420-457, 1982.
  - Proc. IEEE V86N8, 1998 Special issue on MEMS
  - Wu, Micromachining for Optical and Optoelectronic Systems, Proc. IEEE V85N11 pp.1833-1856, 1997.

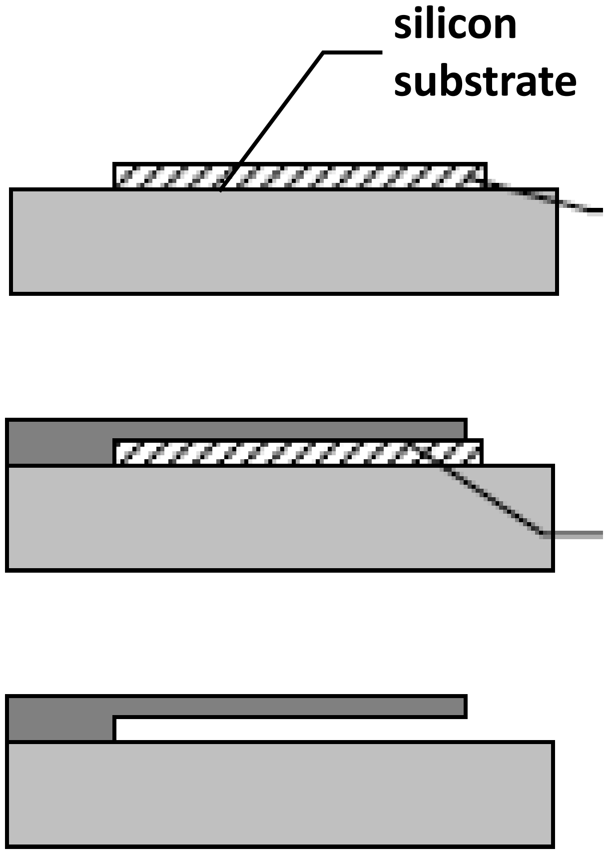
The substrate

- ☐ Explain how single crystalline Si wafers are made
- ☐ Describe the crystalline structure of Si
- ☐ Use wafer flats to identify types of Si wafers
- ☐ Define
  - ☐ **Semiconductor**
  - ☐ **Doping/dopant**
  - ☐ **Resistivity**

Silicon

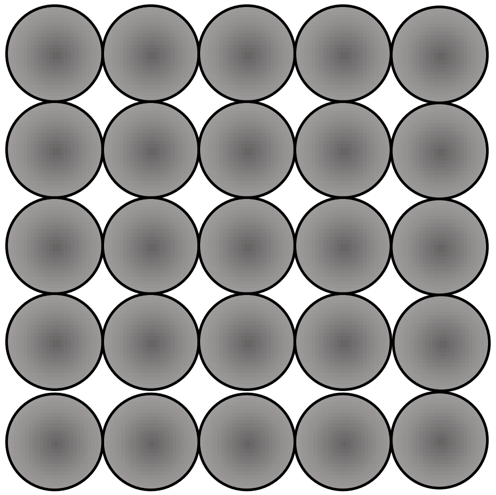


Bulk micromachining



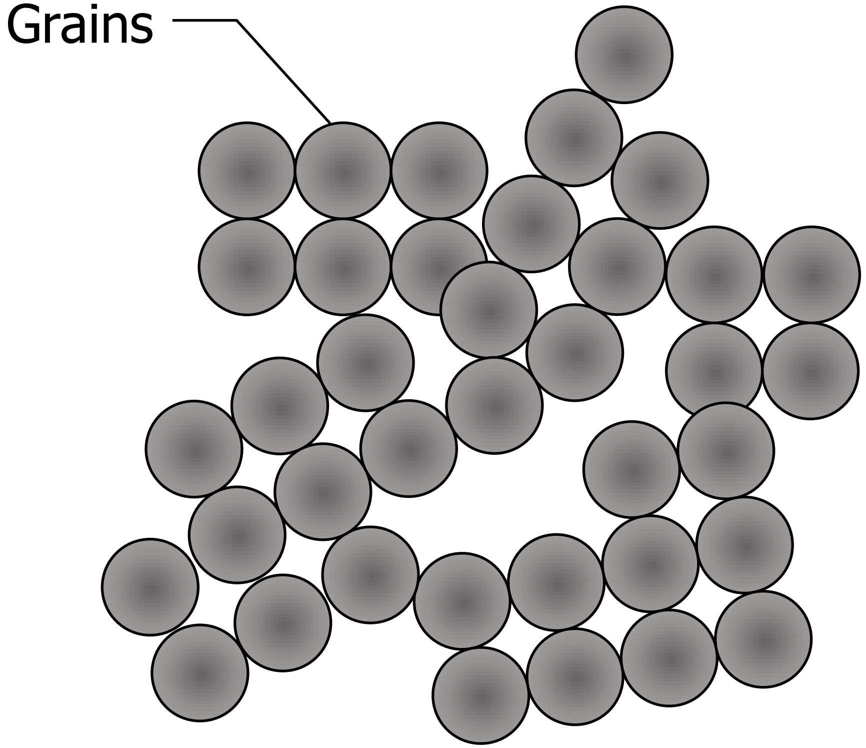
Surface micromachining

Three forms of material



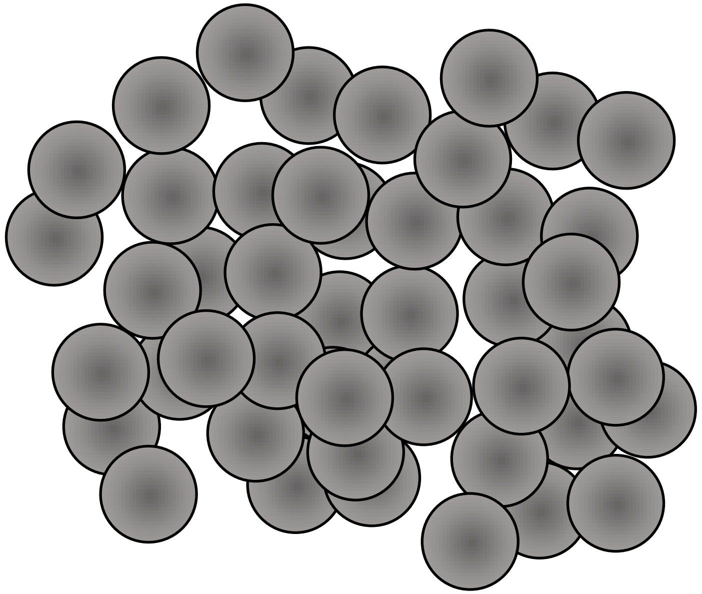
Crystalline

Silicon wafers



Polycrystalline

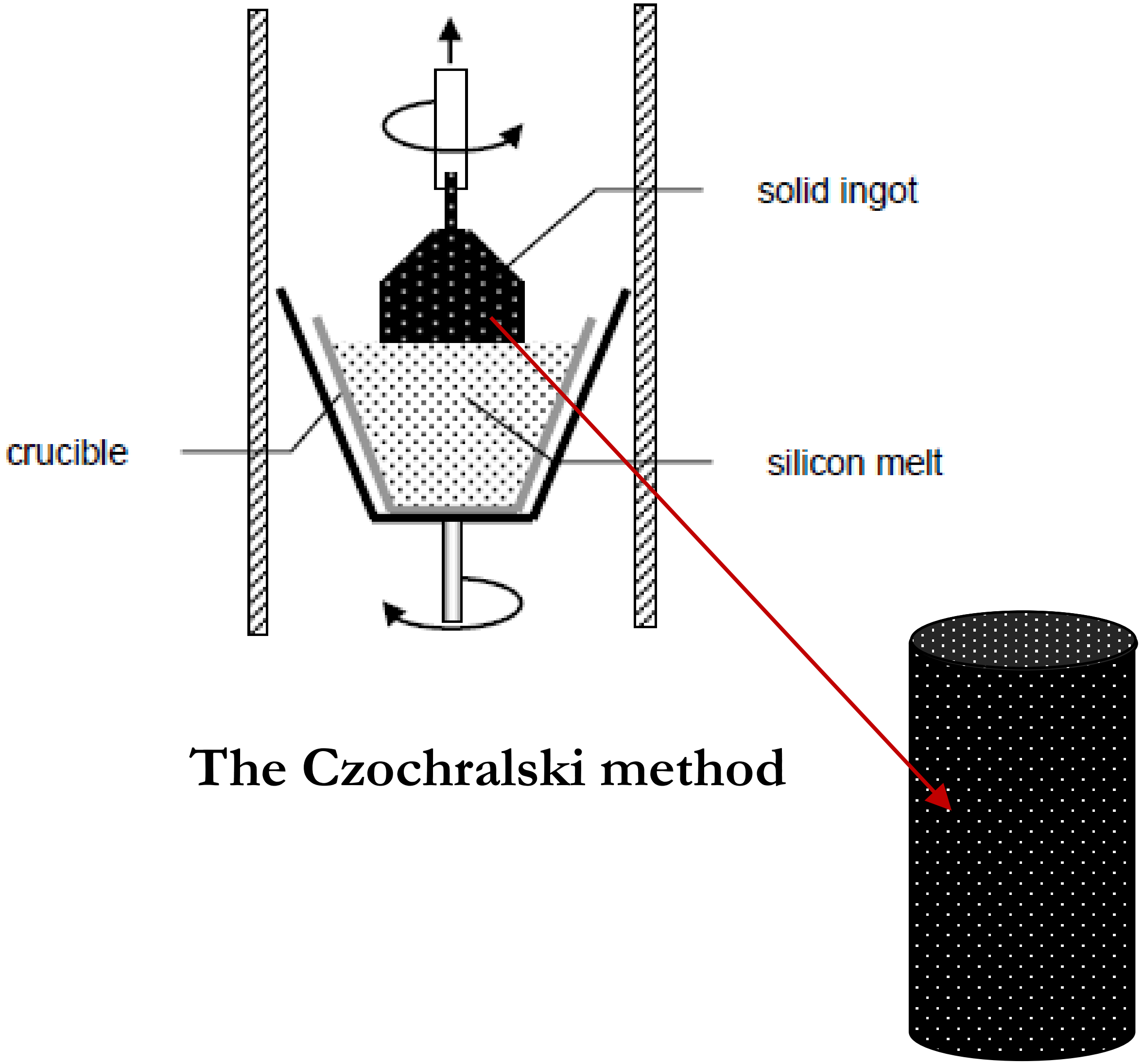
Polysilicon



Amorphous

Glass and fused quartz, polyimide, photoresist

Creating silicon wafers

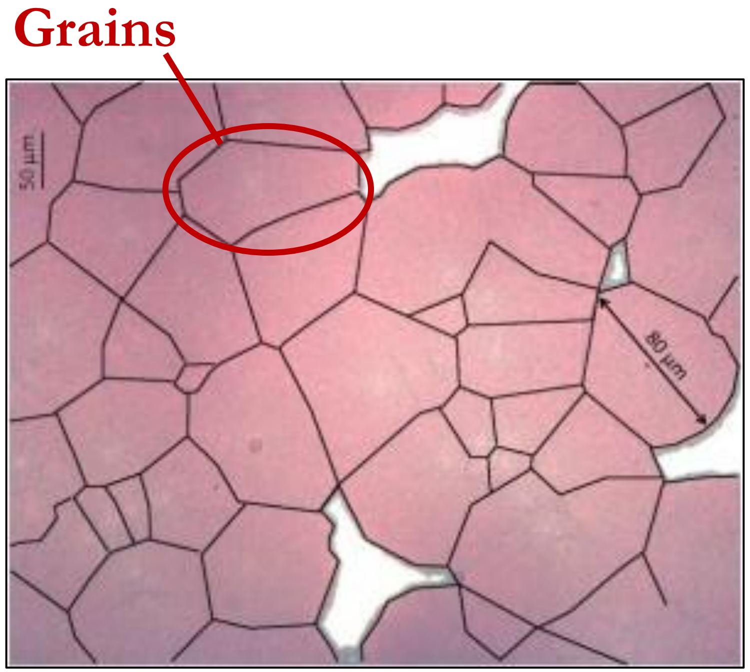


The Czochralski method

- Creates crystalline Si of high purity
- A “seed” of solid Si is placed in molten Si—called the melt—which is then slowly spun and drawn upwards while cooling it.
- Crucible and the “melt” turned in opposite directions
- Wafers cut from the cross section.

Creating silicon wafers

Photo of a monocrystalline silicon ingot

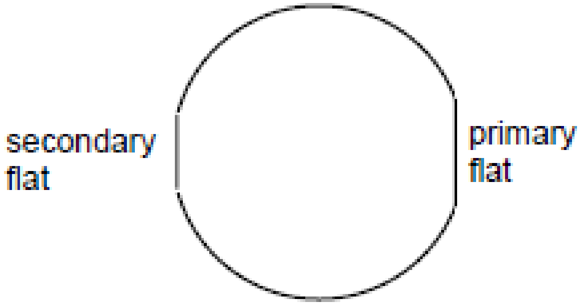


Polycrystalline silicon

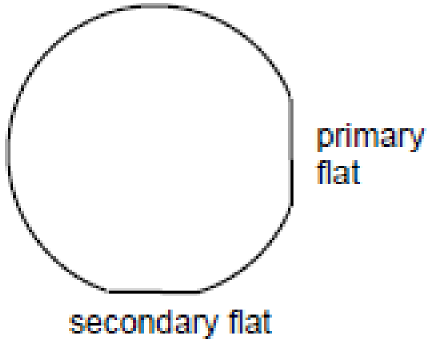
(American Ceramics Society)

Wafer types

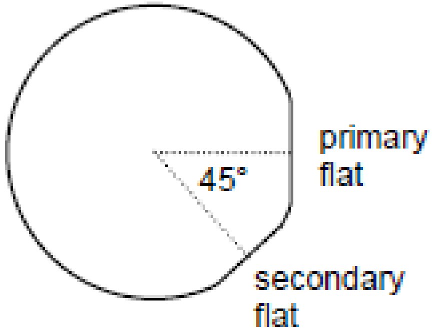
Si wafers differ based on the orientation of their crystal planes in relation to the surface plane of the wafer.



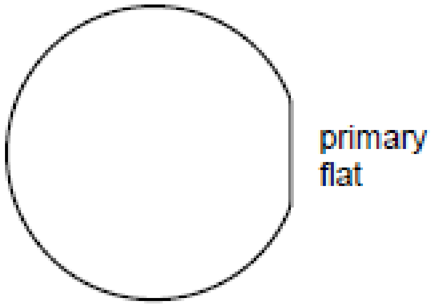
(100) n-type



(100) p-type



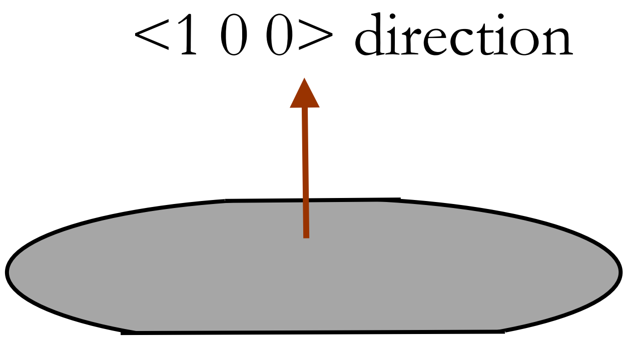
(111) n-type



(111) p-type

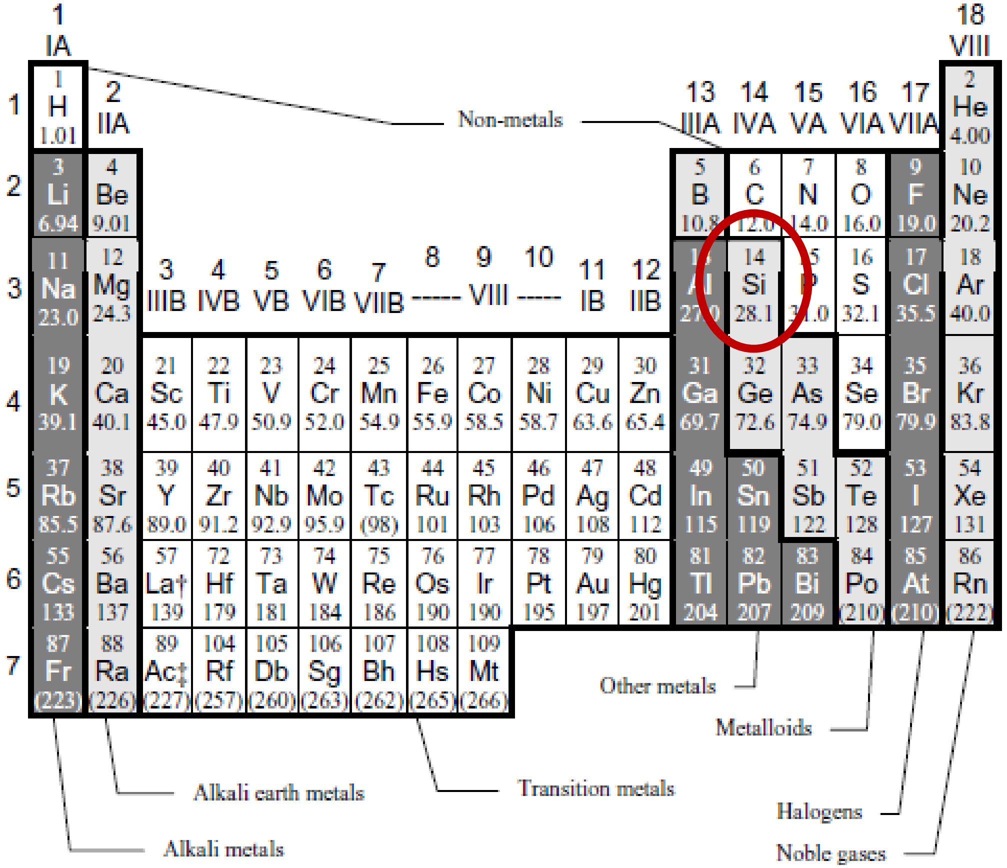
Wafers “flats” are used to identify

- the crystalline orientation of the surface plane, and
- whether the wafer is **n-type** or **p-type**.

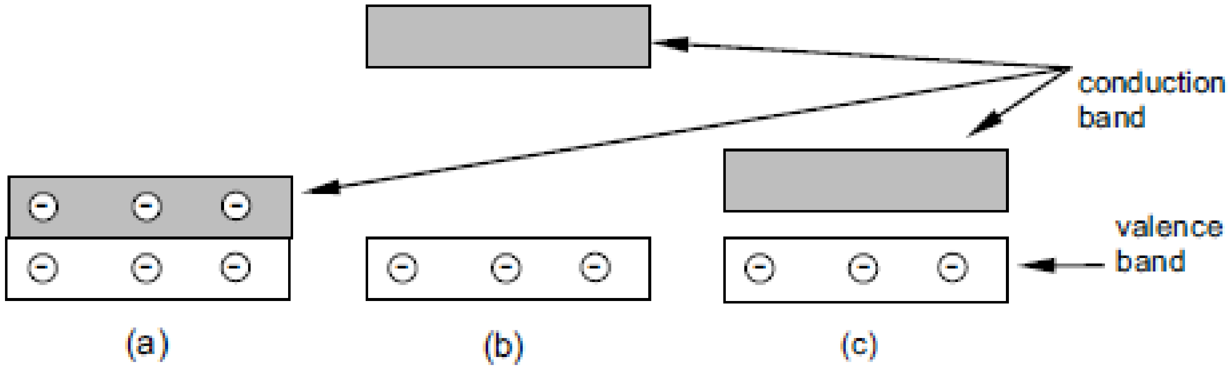


(1 0 0) wafer

It’s a semiconductor



	1 IA	2 IIA	3 IIIB	4 IVB	5 VB	6 VIB	7 VIIB	8	9 VIII	10	11 IB	12 IIB	13 IIIA	14 IVA	15 VA	16 VIA	17 VIIA	18 VIII
1	1 H 1.01																	2 He 4.00
2	3 Li 6.94	4 Be 9.01											5 B 10.8	6 C 12.0	7 N 14.0	8 O 16.0	9 F 19.0	10 Ne 20.2
3	11 Na 23.0	12 Mg 24.3											13 Al 27.0	14 Si 28.1	15 P 31.0	16 S 32.1	17 Cl 35.5	18 Ar 40.0
4	19 K 39.1	20 Ca 40.1	21 Sc 45.0	22 Ti 47.9	23 V 50.9	24 Cr 52.0	25 Mn 54.9	26 Fe 55.9	27 Co 58.5	28 Ni 58.7	29 Cu 63.6	30 Zn 65.4	31 Ga 69.7	32 Ge 72.6	33 As 74.9	34 Se 79.0	35 Br 79.9	36 Kr 83.8
5	37 Rb 85.5	38 Sr 87.6	39 Y 89.0	40 Zr 91.2	41 Nb 92.9	42 Mo 95.9	43 Tc (98)	44 Ru 101	45 Rh 103	46 Pd 106	47 Ag 108	48 Cd 112	49 In 115	50 Sn 119	51 Sb 122	52 Te 128	53 I 127	54 Xe 131
6	55 Cs 133	56 Ba 137	57 La† 139	72 Hf 179	73 Ta 181	74 W 184	75 Re 186	76 Os 190	77 Ir 190	78 Pt 195	79 Au 197	80 Hg 201	81 Tl 204	82 Pb 207	83 Bi 209	84 Po (210)	85 At (210)	86 Rn (222)
7	87 Fr (223)	88 Ra (226)	89 Ac‡ (227)	104 Rf (257)	105 Db (260)	106 Sg (263)	107 Bh (262)	108 Hs (265)	109 Mt (266)									



(a) Conductors

(b) Insulators

(c) Semiconductors

The “jump” is affected by both temperature and light → sensors and optical switches

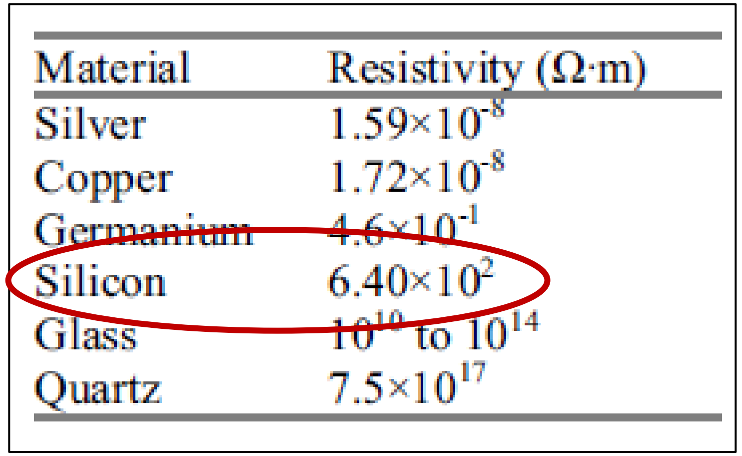
Conductivity, resistivity, and resistance

Electrical conductivity (σ) →

- A measure of how easily a material conducts electricity
- Material property

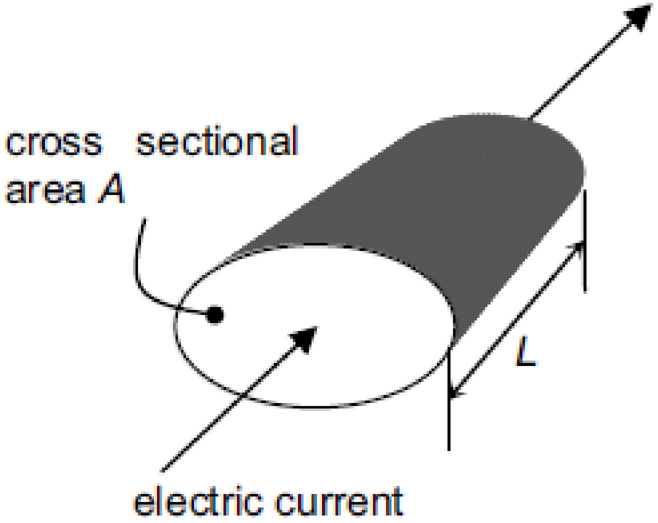
Electrical resistivity (ρ) →

- Inverse of conductivity; $\rho = 1/\sigma$
- Material property



Material	Resistivity (Ω·m)
Silver	1.59×10^{-8}
Copper	1.72×10^{-8}
Germanium	4.6×10^{-1}
Silicon	6.40×10^{2}
Glass	10^{10} to 10^{14}
Quartz	7.5×10^{17}

By **doping**, the resistivity of silicon can be varied over a range of about 1×10^{-4} to 1×10^{8} Ω•m!



$$R = \frac{L}{\sigma A} = \rho \frac{L}{A}$$

Conductivity, resistivity, and resistance

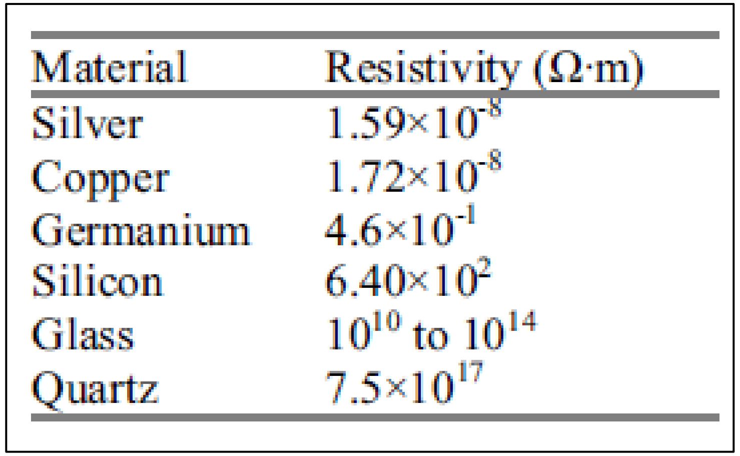
Quiz

Find the total resistance (in Ω) for the MEMS snake resistor shown in the figure if it is made of

- Aluminum (ρ = 2.52×10^{-8} Ω·m) and
- Silicon

Answers:

- Al: 509 Ω
- Si: 1.3 GΩ !!



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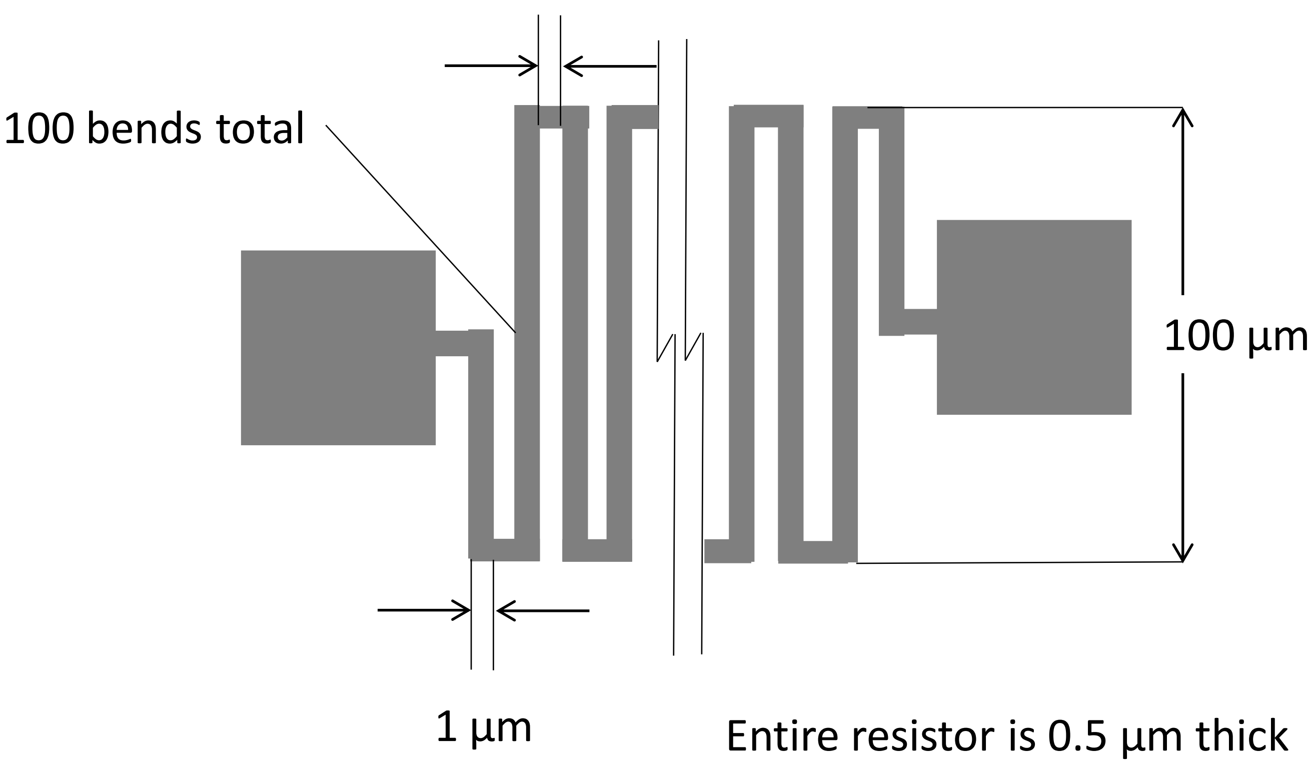
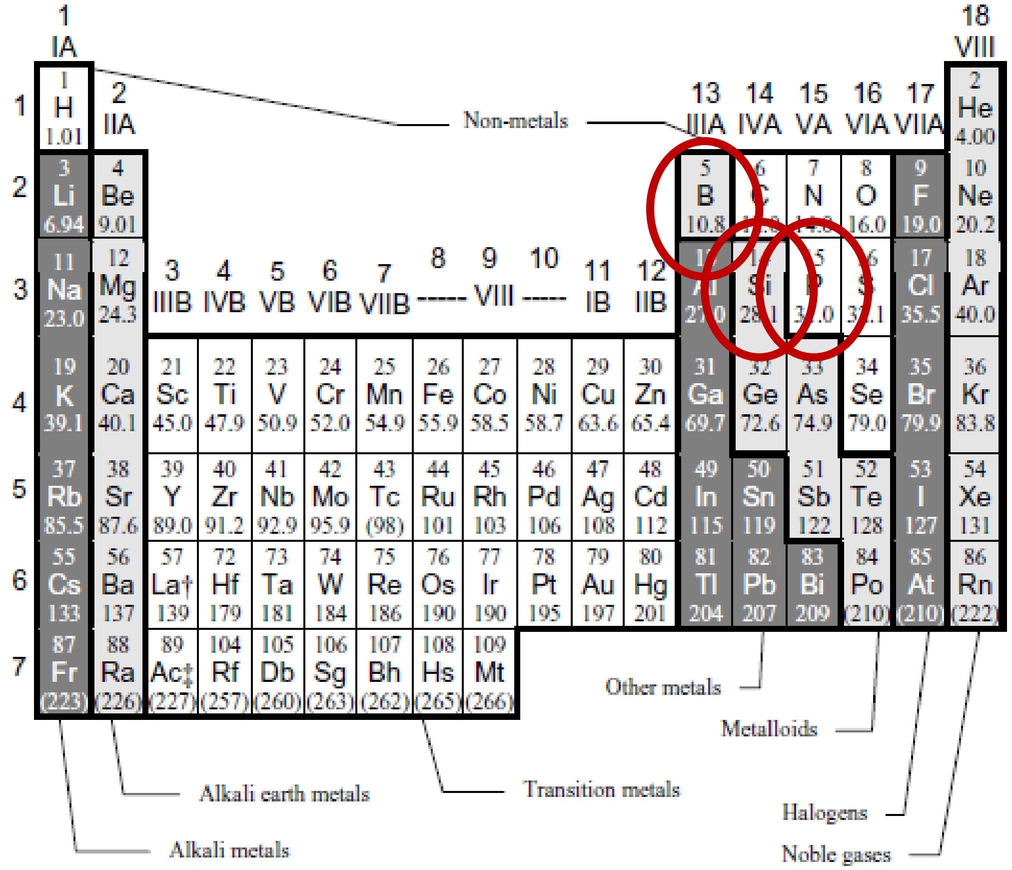


Entire resistor is 0.5 µm thick

Doping



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(a) Phosphorus is a **donor** – donates electrons

(b) Boron is an **acceptor** – accepts electrons from Si

→ Charge carriers are “holes.”

Phosphorus and boron are both **dopants**.

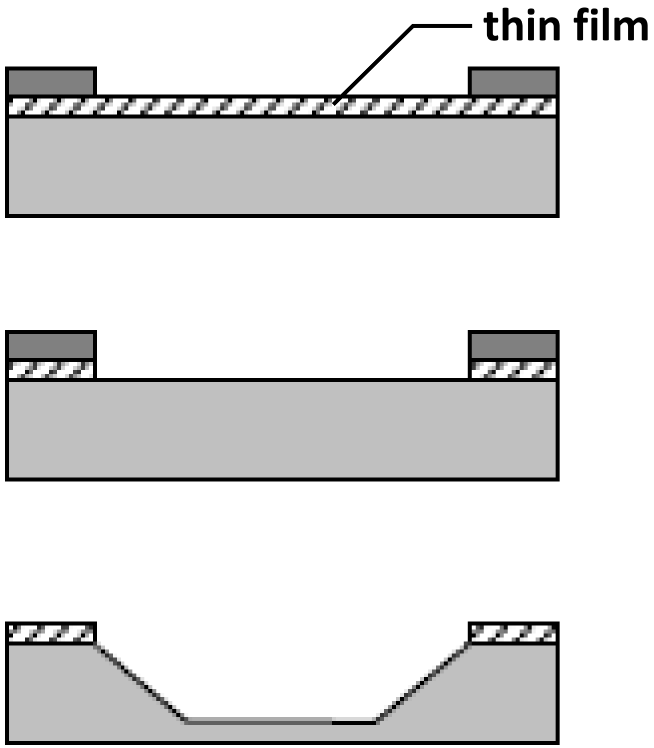
P creates an **n-type** semiconductor.

B creates a **p-type** semiconductor.

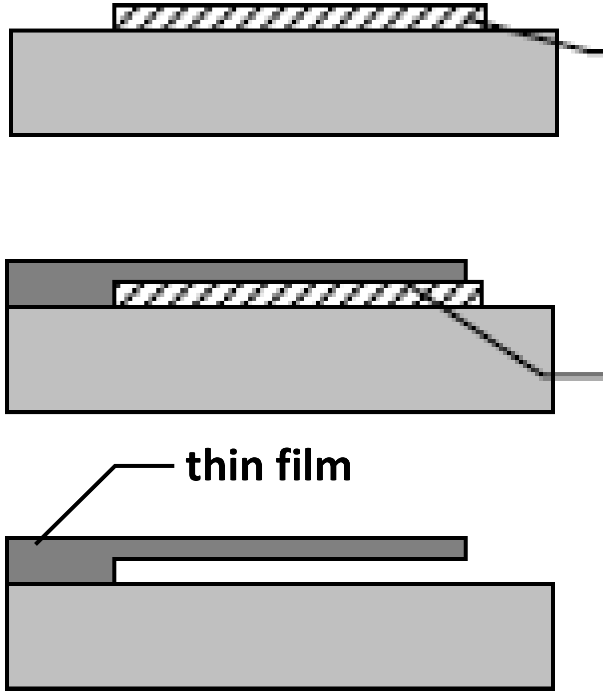
Working on Substrate - Step 2

- ☐ Describe the processes of
  - ☐ Oxidation, both
    - ☐ dry oxidation and
    - ☐ wet oxidation
  - ☐ Evaporation, both
    - ☐ resistive reheating and
    - ☐ e-beam
  - ☐ Sputtering,
    - ☐ DC,
    - ☐ RF,
    - ☐ reactive, and
    - ☐ magnetron
  - ☐ Chemical vapor deposition (CVD)
  - ☐ Electrodeposition
  - ☐ Spin casting
- ☐ Calculate
  - ☐ relative thicknesses of added oxide layers to original wafer thickness
- ☐ Compare and contrast the advantages and disadvantages of evaporation versus sputtering
- ☐ Give the relative advantages and disadvantages of CVD compared to PVD

Adding layers to the silicon substrate



Bulk micromachining



Surface micromachining

Adding layers to the substrate

Many different methods

- **Epitaxy**—growing an additional crystalline layer of Si on top of an existing wafer
  - Has same crystalline orientation of underlying Si (unless it is on top of an **amorphous** substrate, in which case it is **polycrystalline**)
  - Has different **dopant** type and concentration
  - Uses?
- **Oxidation**—chemical reaction of Si with O_2 to form layer of **amorphous** silicon dioxide (SiO_2)

- **Evaporation**
- **Sputtering**

Physical vapor deposition (**PVD**)

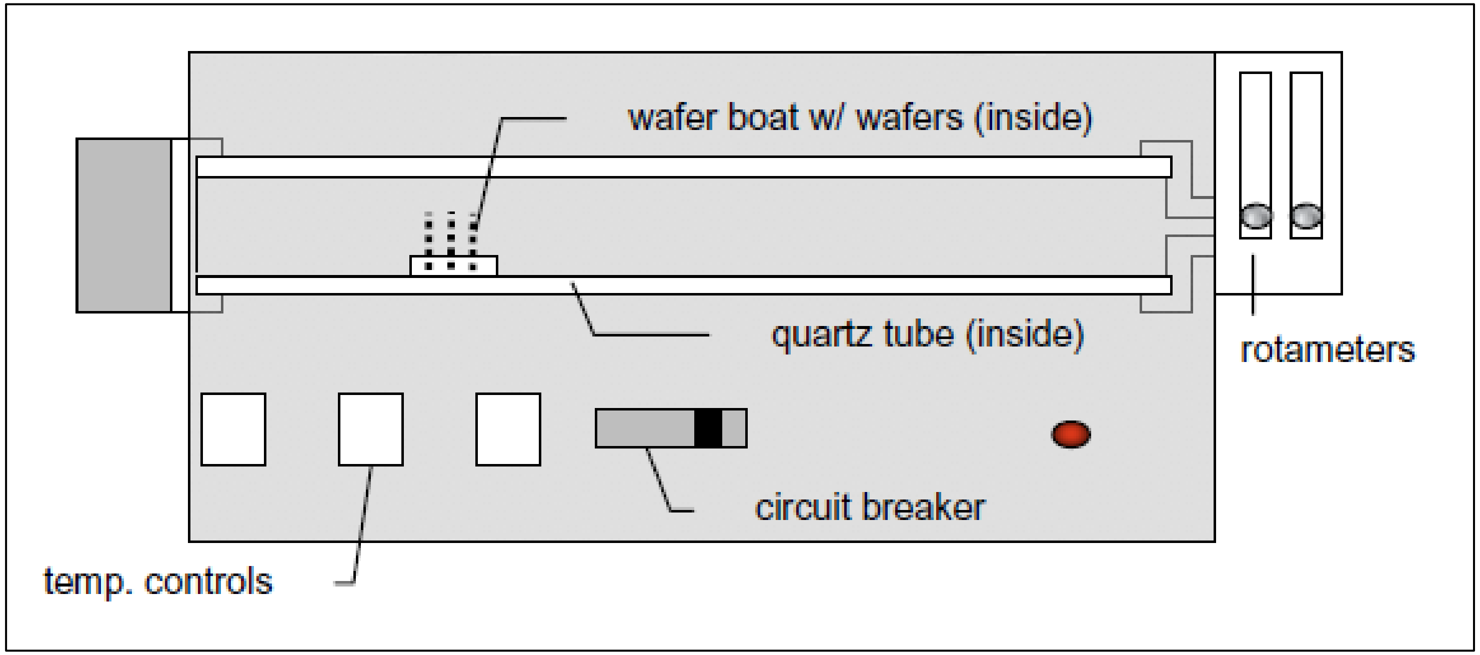
- **Chemical vapor deposition** (**CVD**)
- **Electrodeposition**
- **Spin casting**

Oxidation

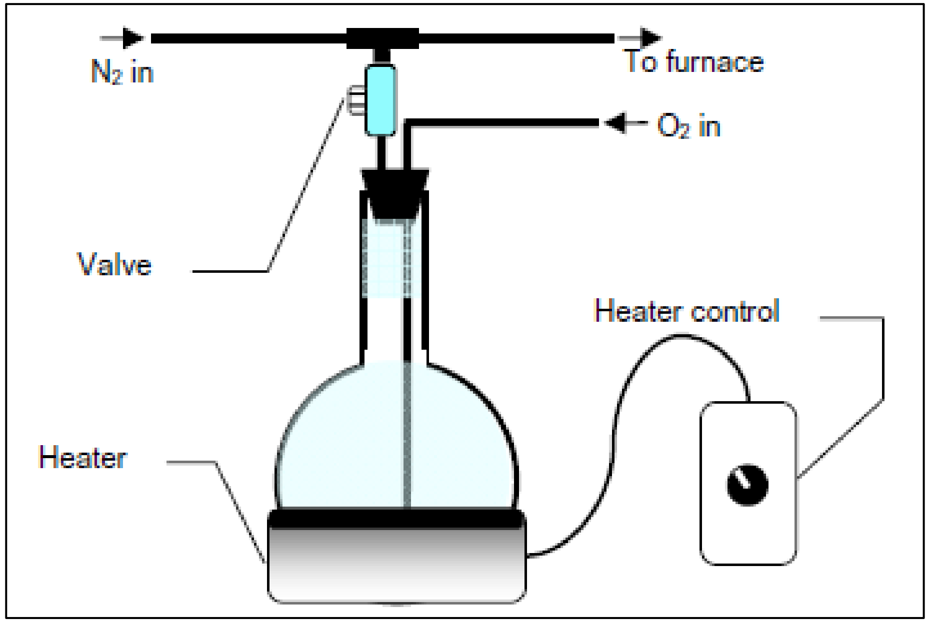
Chemical reaction of Si with O_2 to form layer of **amorphous** silicon dioxide (SiO_2)

- Called “oxide layer” or just “oxide”
- Uses?
- Thin layers < 100 nm
- Thick layers 100 nm – 1.5 µm
- Use of furnaces at high temperatures, ~800°-1200°C

Oxidation furnaces



A schematic diagram of a typical oxidation furnace



“Bubblers” (bubble) are used for wet oxidation.

Wet oxidation vs. dry oxidation

Oxidation can be **dry** or **wet**.

Dry oxidation:

$Si + O_2 \rightarrow$

Dry oxidation creates a very high quality oxide, but it takes a long time.

Wet oxidation:

$Si + H_2O \rightarrow$

Wet oxidation creates a lower quality oxide, but it is fast.

Oxidation

$$\boxed{\frac{x_{add}}{x_{ox}} = 0.54}$$

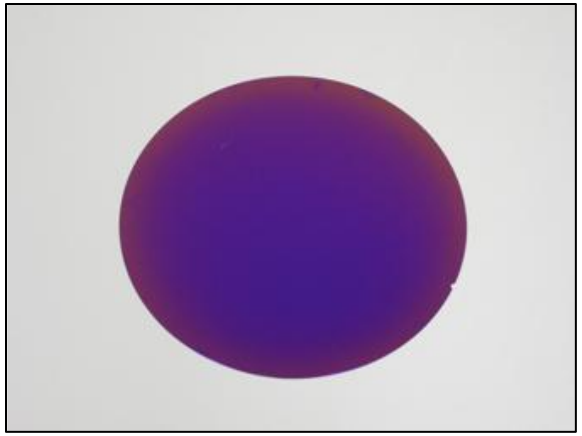
A 150-mm (6 inch) diameter silicon wafer requires a 0.8-µm thick layer of oxide as a sacrificial layer. If the wafer is originally 650 mm thick, how much thicker is the wafer after oxidation? How much of the wafer has been “used up” to create the oxide later?

Answer:

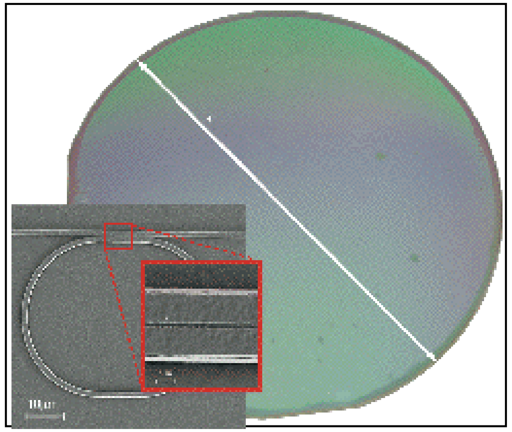
- 0.43 µm thicker (total thickness = 650.43 µm)
- 0.37 µm of wafer “used up”

Oxide thickness

How can you tell how thick your oxide layer is? → Look at the color!



(www.filmetrics.com)



(onlinelibrary.wiley.com)

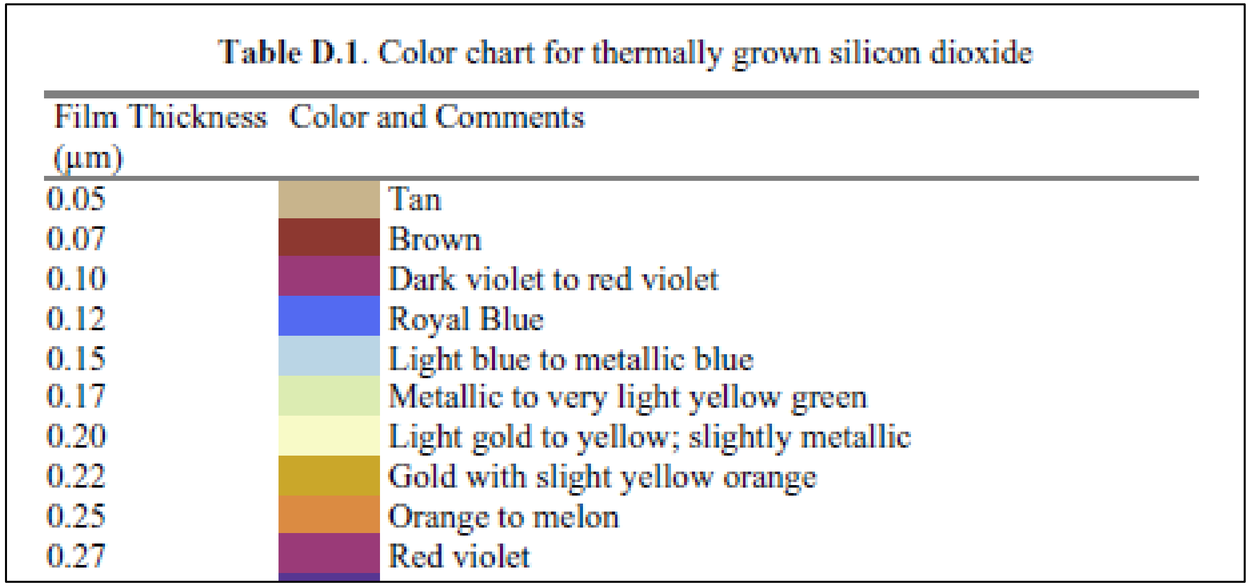
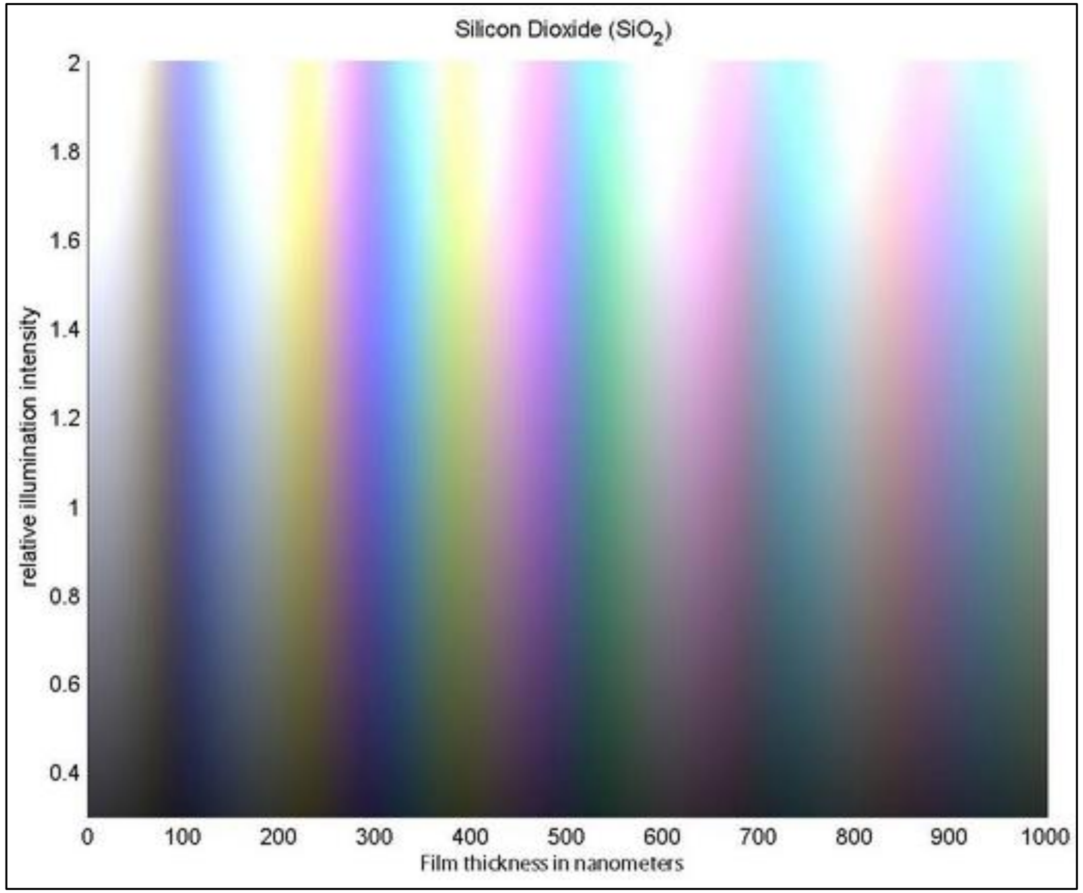


Table D.1. Color chart for thermally grown silicon dioxide

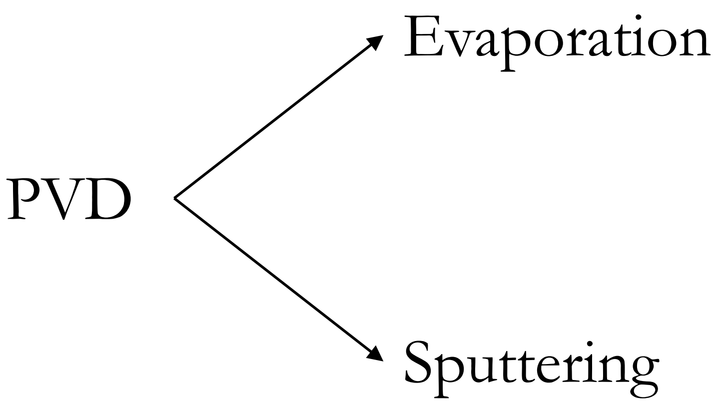
Film Thickness (μm)	Color and Comments	
0.05	🟫	Tan
0.07	🟫	Brown
0.10	🟪	Dark violet to red violet
0.12	🟦	Royal Blue
0.15	🟦	Light blue to metallic blue
0.17	🟩	Metallic to very light yellow green
0.20	🟨	Light gold to yellow; slightly metallic
0.22	🟨	Gold with slight yellow orange
0.25	🟧	Orange to melon
0.27	🟪	Red violet



(www.cleanroom.byu.edu)

Physical vapor deposition

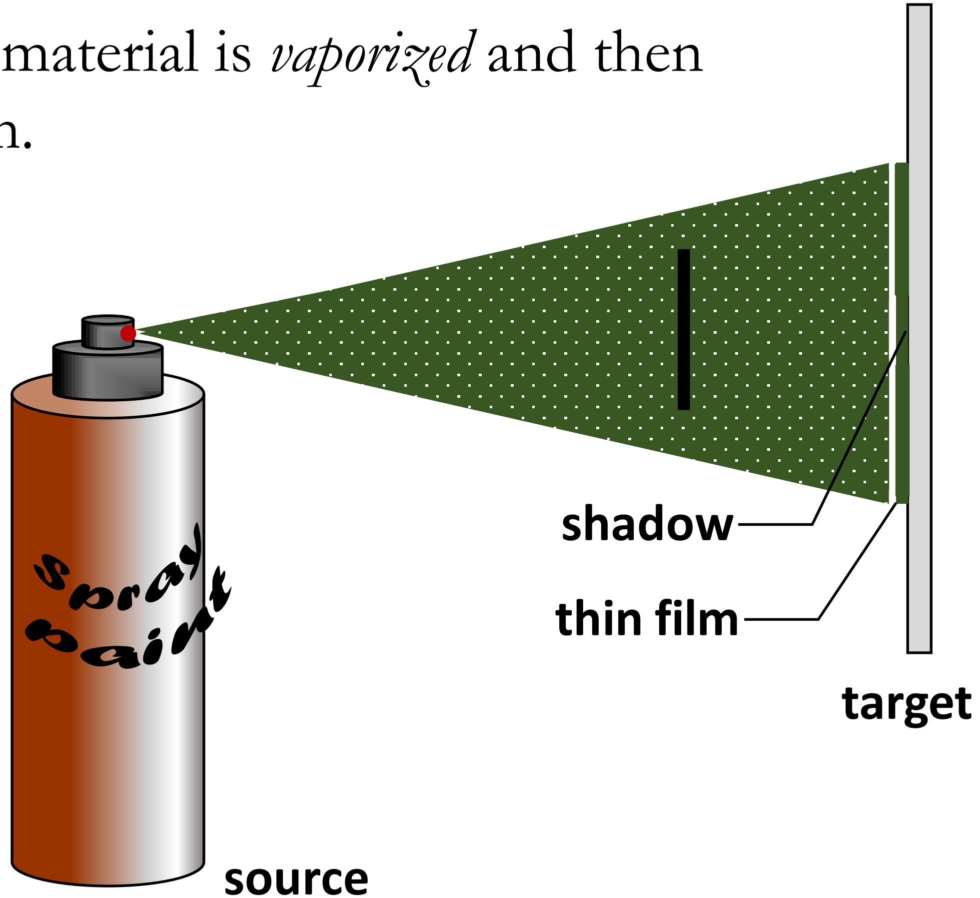
Physical vapor deposition (PVD) – a purified, solid material is *vaporized* and then *condensed* onto a substrate in order to form a thin film.



PVD

Evaporation

Sputtering



PVD is called a **line-of-sight** method. → Shadowing

Vacuums

PVD requires the use of a **vacuum**.

Write down some reasons why you think a vacuum is necessary for PVD.

- Vaporized atoms do not run into other gas atoms
- Need a vacuum to create a vapor out of the source material
- Vacuum helps keep contaminants from being deposited on the substrate

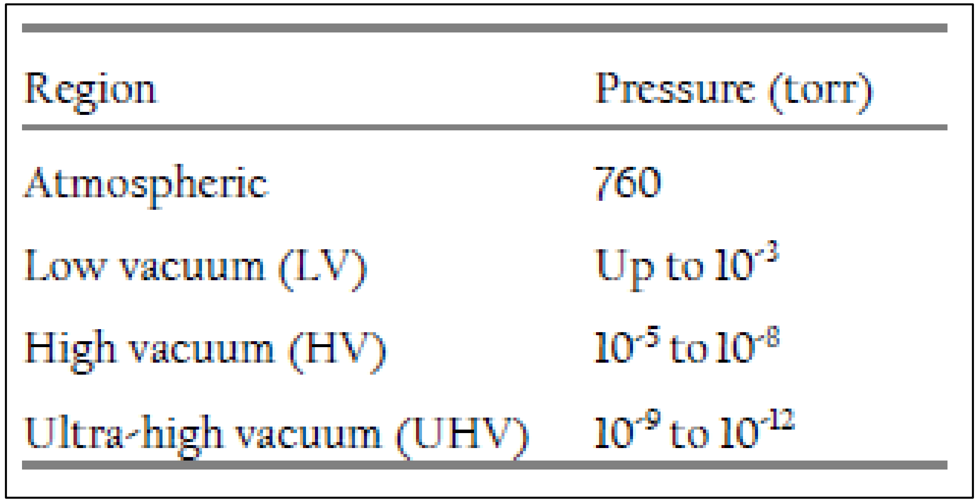
Vacuum fundamentals

Vacuum means pressure less than atmospheric pressure.

Standard unit is a **torr**:

$$1 \text{ atm} = 1.01325\times10^{5} \text{ Pa} = 760 \text{ torr}$$

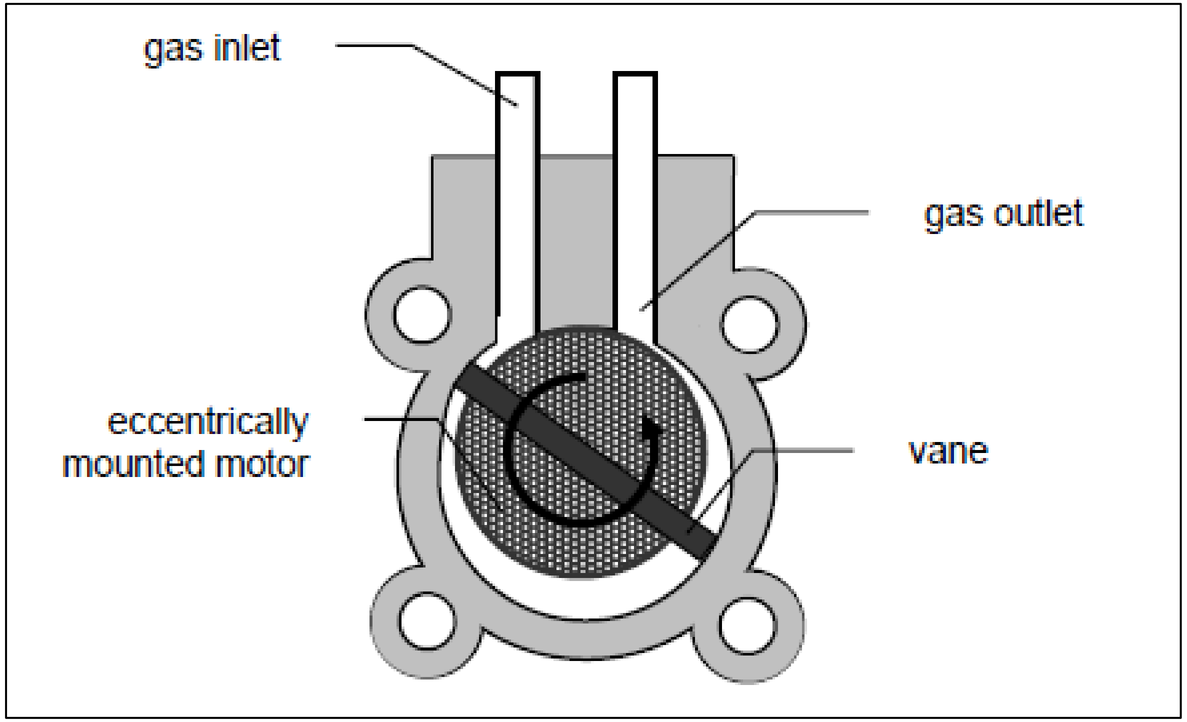
Pressure ranges for various vacuum regions



Region	Pressure (torr)
Atmospheric	760
Low vacuum (LV)	Up to 10^{-3}
High vacuum (HV)	10^{-5} to 10^{-8}
Ultra-high vacuum (UHV)	10^{-9} to 10^{-12}

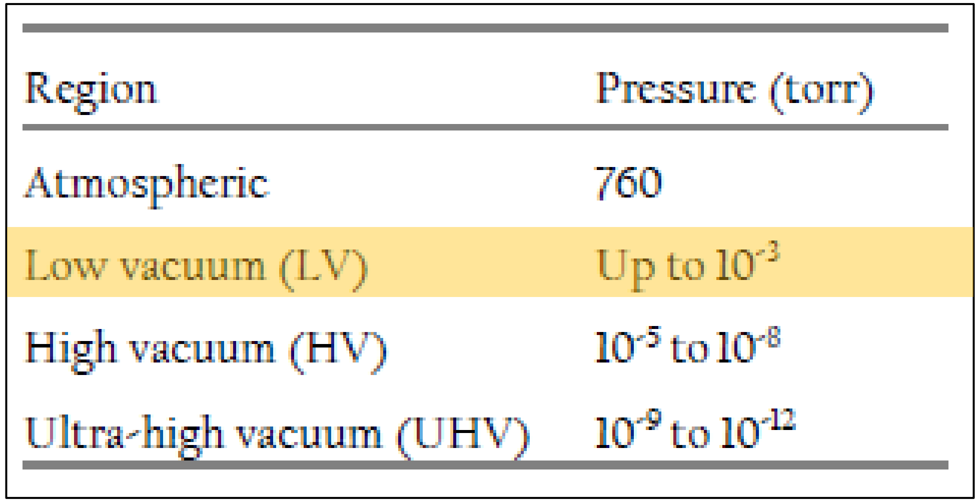
Creating a vacuum

Vacuum pumps



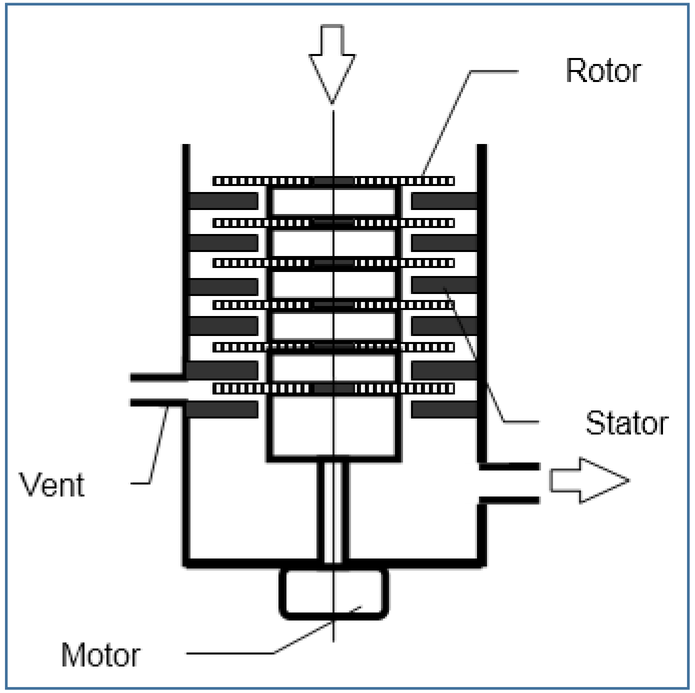
A rotary vane pump

Pressure ranges for various vacuum regions

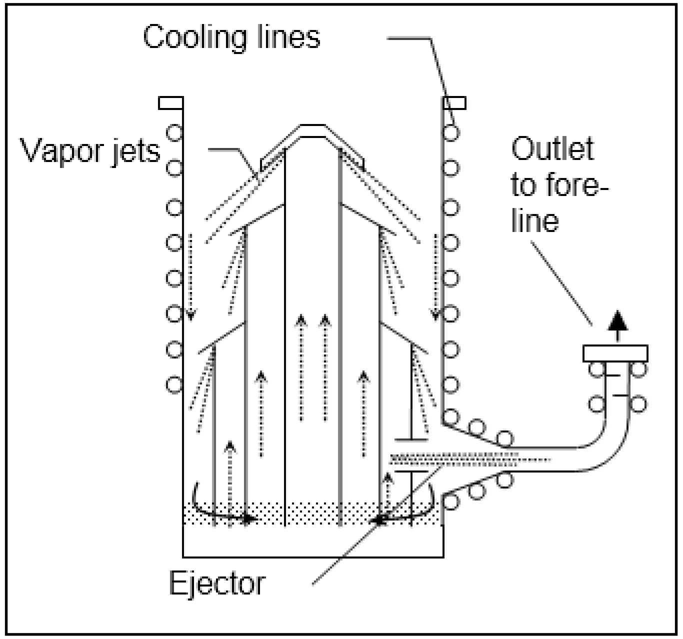


Region	Pressure (torr)
Atmospheric	760
Low vacuum (LV)	Up to 10^{-3}
High vacuum (HV)	10^{-5} to 10^{-8}
Ultra-high vacuum (UHV)	10^{-9} to 10^{-12}

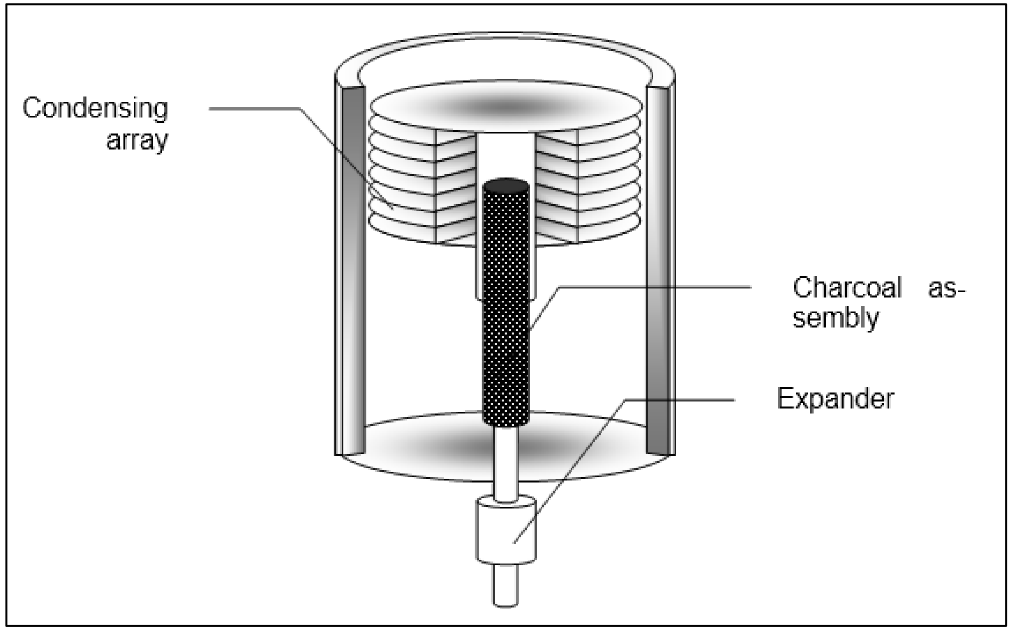
High vacuum pumps



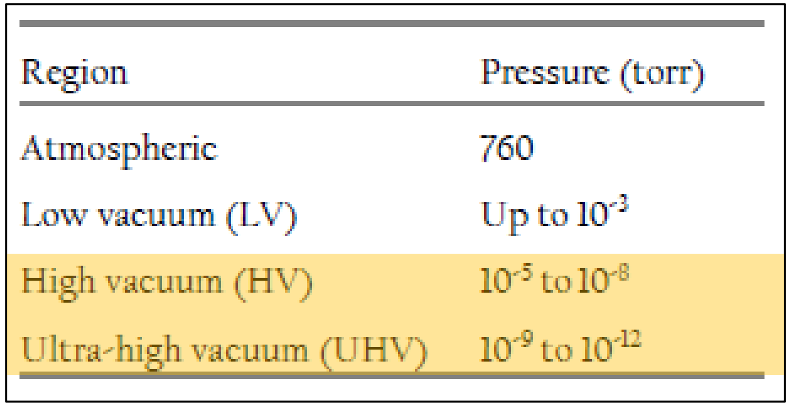
Turbopump



Diffusion pump

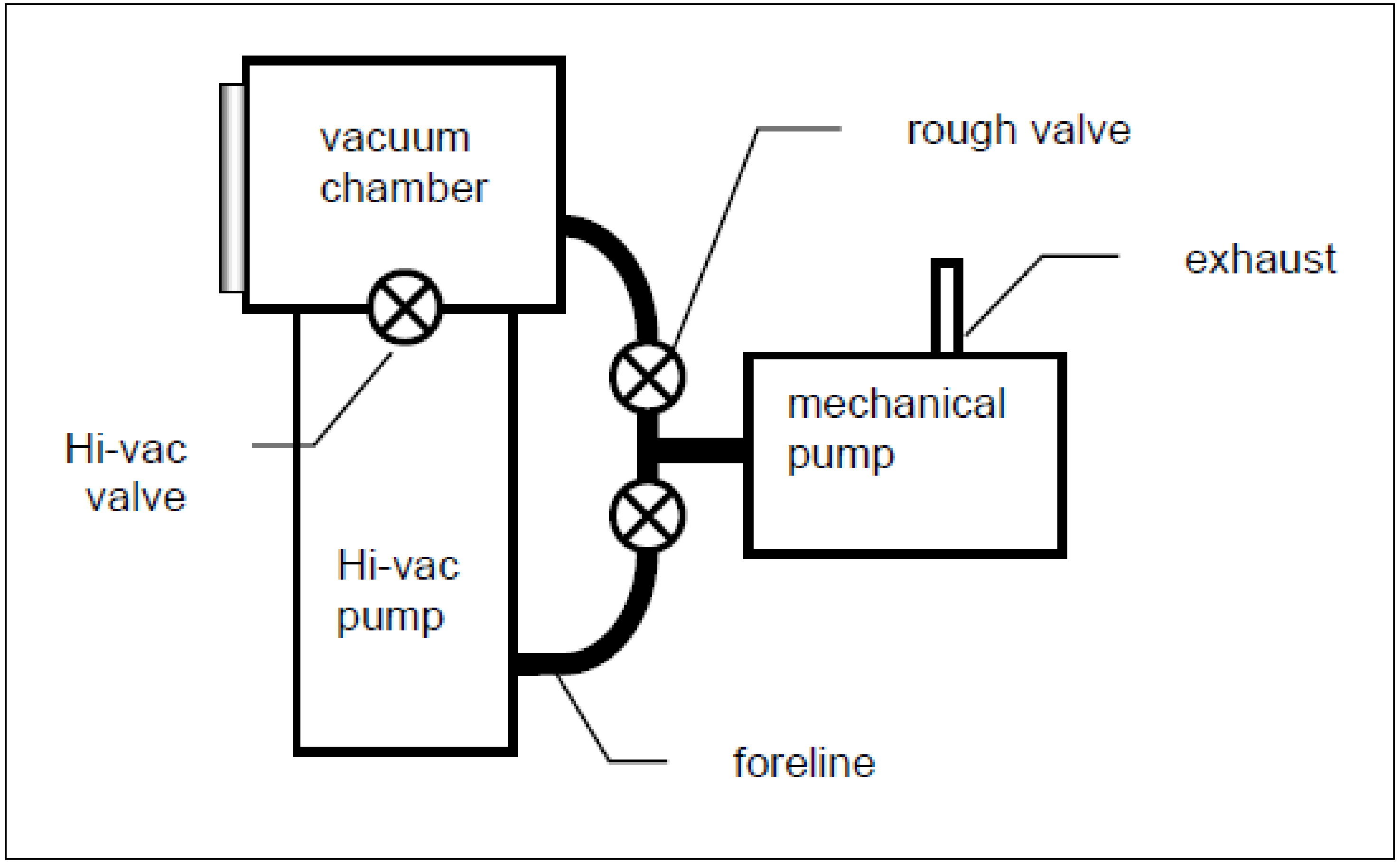


Cryopump



Region	Pressure (torr)
Atmospheric	760
Low vacuum (LV)	Up to 10^{-3}
High vacuum (HV)	10^{-5} to 10^{-8}
Ultra-high vacuum (UHV)	10^{-9} to 10^{-12}

Vacuum systems

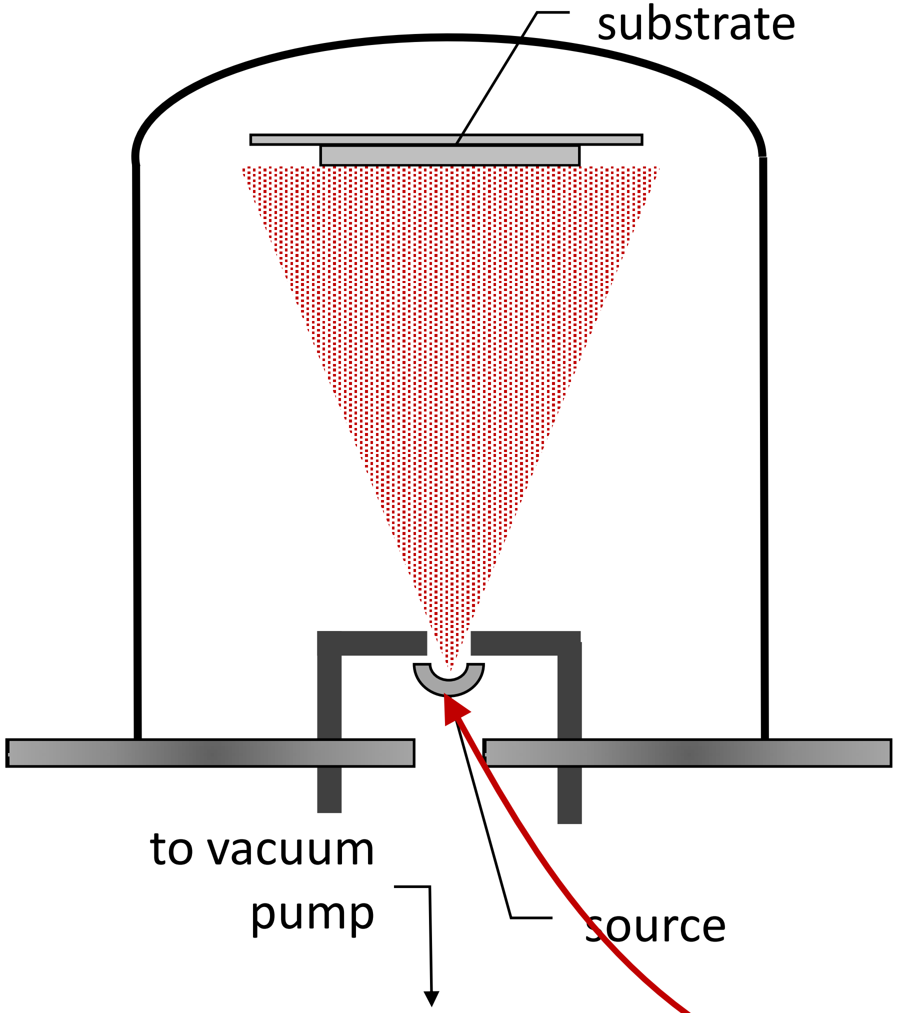


Typical vacuum system setup in a PVD system

In what order would you operate the pumps and open and close valves to create a high vacuum in the vacuum chamber?

1. Close Hi-vac and foreline valves
2. Run the "rough pump" to lower chamer to low vacuum
3. Close rough valve
4. Open foreline valve
5. Open Hi-vac valve
6. Run Hi-vac pump

Thermal evaporation



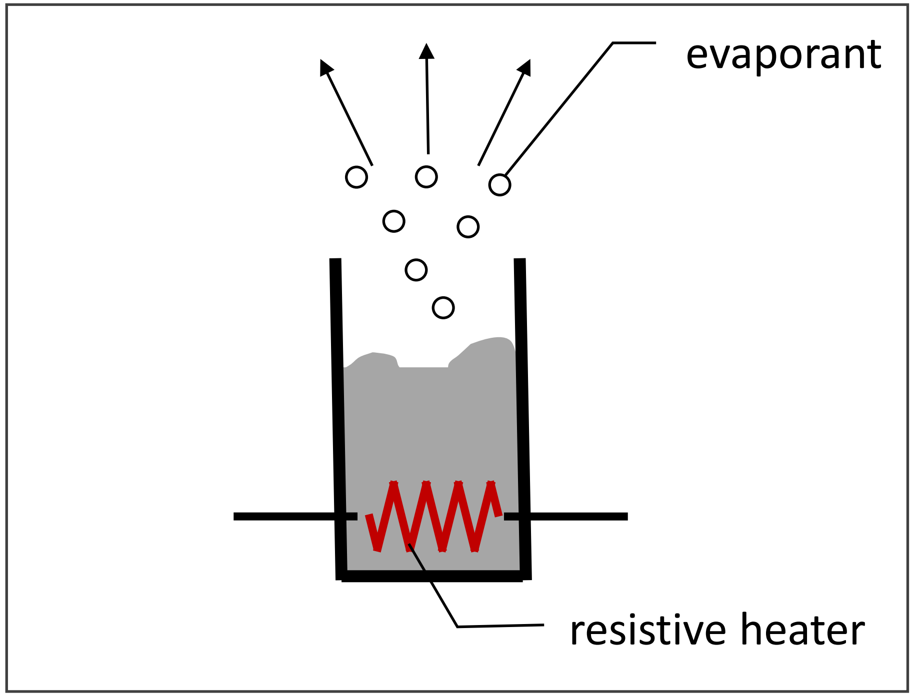
Flux, F: (molecules leaving source)/(area×time)

$$F = \frac{P_v(T)}{\sqrt{2\pi M k_b T}}$$

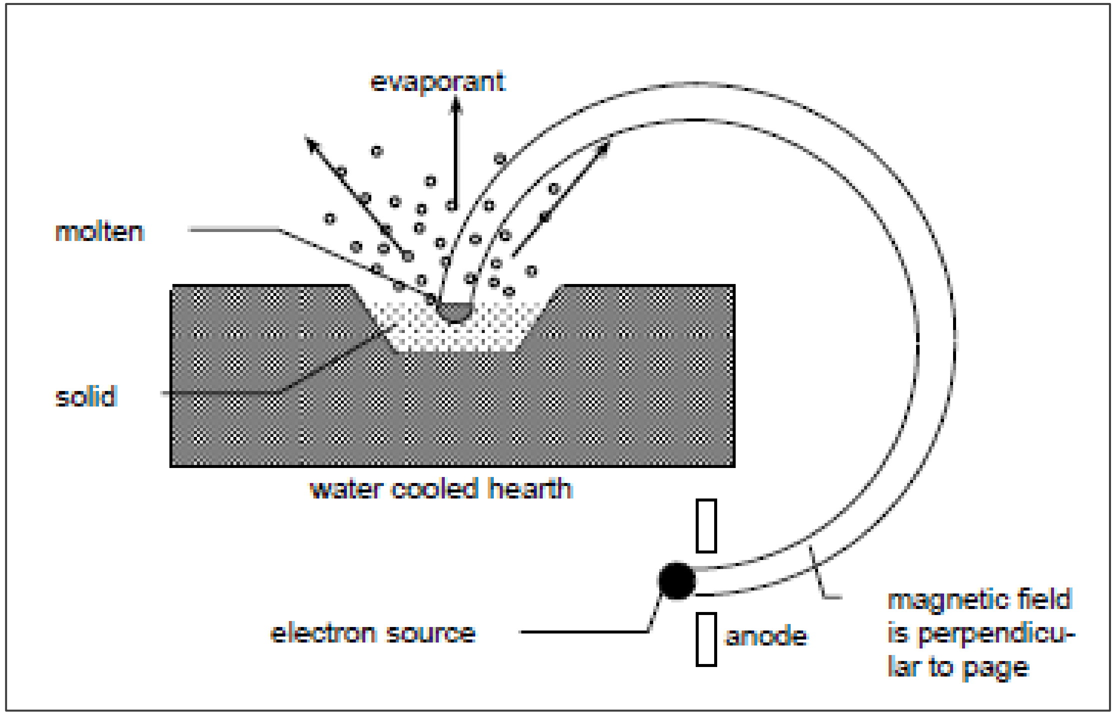
Requirements for evaporated materials:

- P_v must be > background vacuum pressure, ~ 10^{-2} torr < P_v < 1
- Elements or simple oxides of elements
- $600^{\circ}\mathrm{C} < T < 1200^{\circ}\mathrm{C}$
- Examples Al, Cu, Ni, ZiO
- No heavy metals; e.g. Pt, Mo, Ta, and W

Resistive heating vs. e-beam evaporation

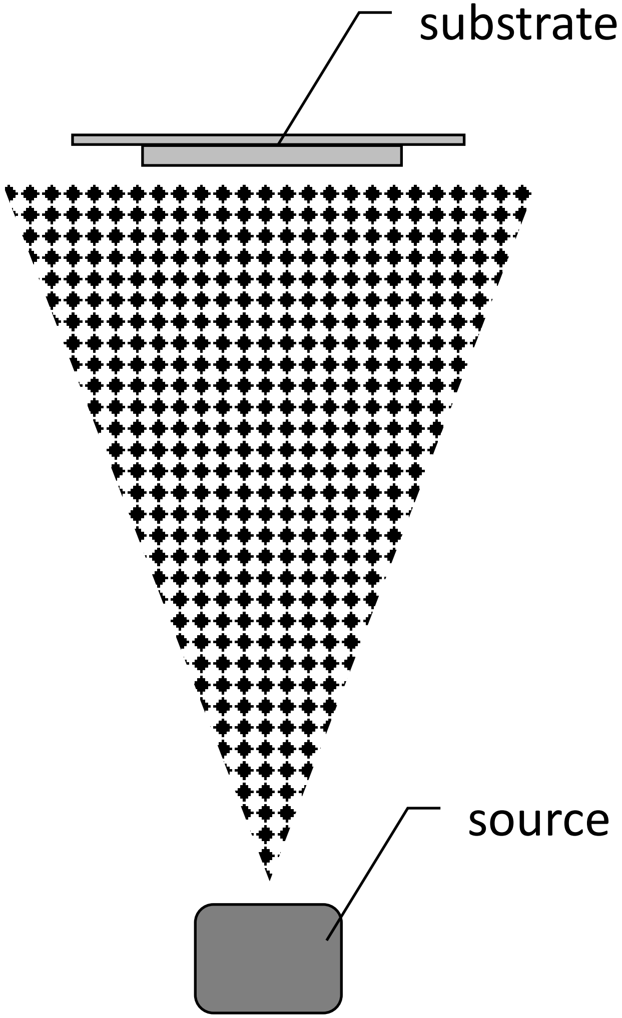


Evaporation by resistive heating

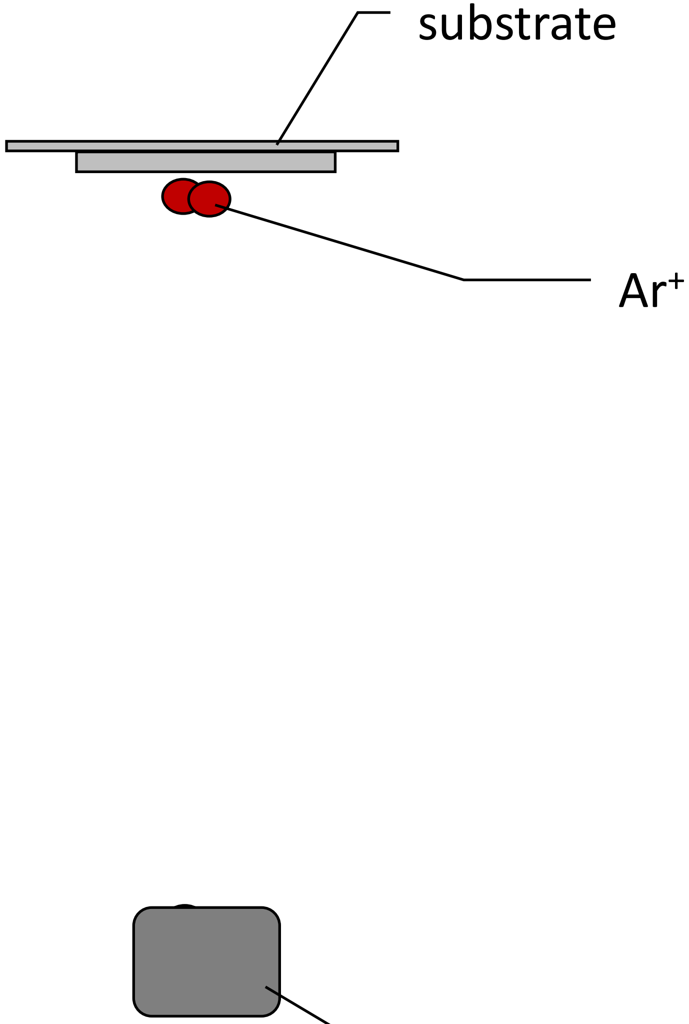


e-beam evaporation

Sputtering

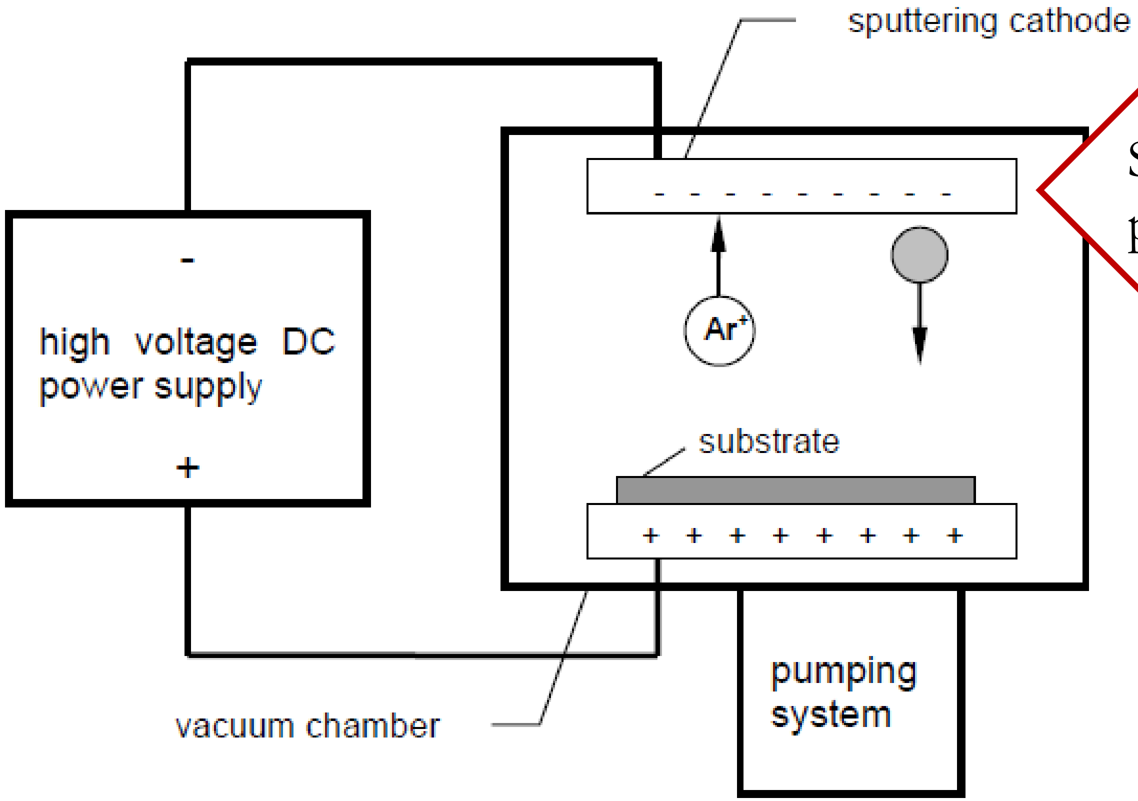


Evaporation



Sputtering

DC sputtering



Source is not a “point” but a parallel plate.

Source material must be *conductive*

Typical DC sputtering configuration

Other sputtering techniques

RF (radio frequency) Sputtering

- Applies an AC voltage to target at frequencies > 50 Hz
- Target does not need to be conductive
- Chamber walls also sputtered

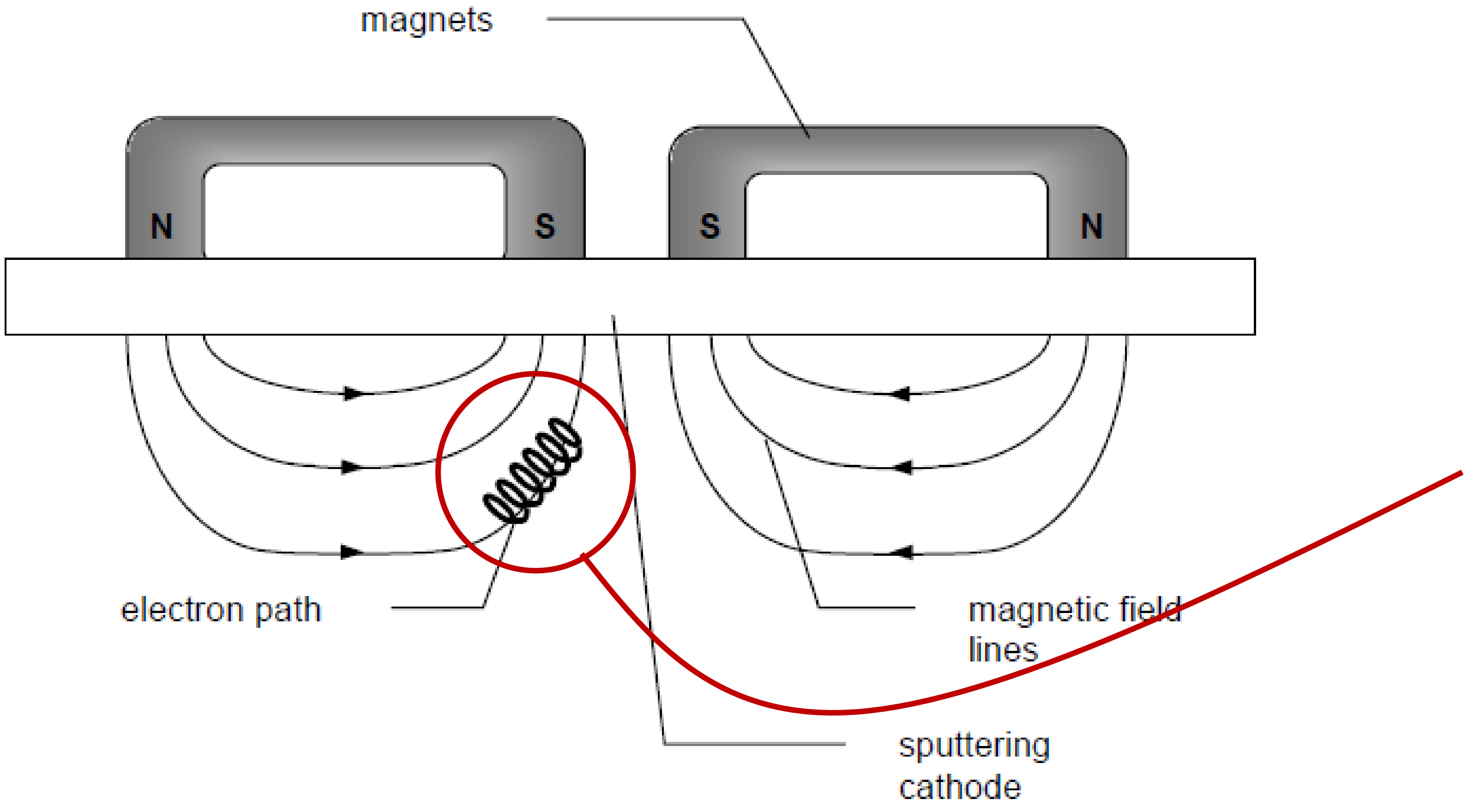
Reactive sputtering

- Reactive gas (such as O_2) added to chamber
- Reacts with target, products forming the deposited materials
- Products can be deposited on surfaces other than the substrate
- Reduction in sputtering rates typically seen

Magnetron sputtering

- Addition of magnets behind target keep electrons from travelling too far
- Increased ionization at cathode
- Leads to higher yields

Magnetron sputtering



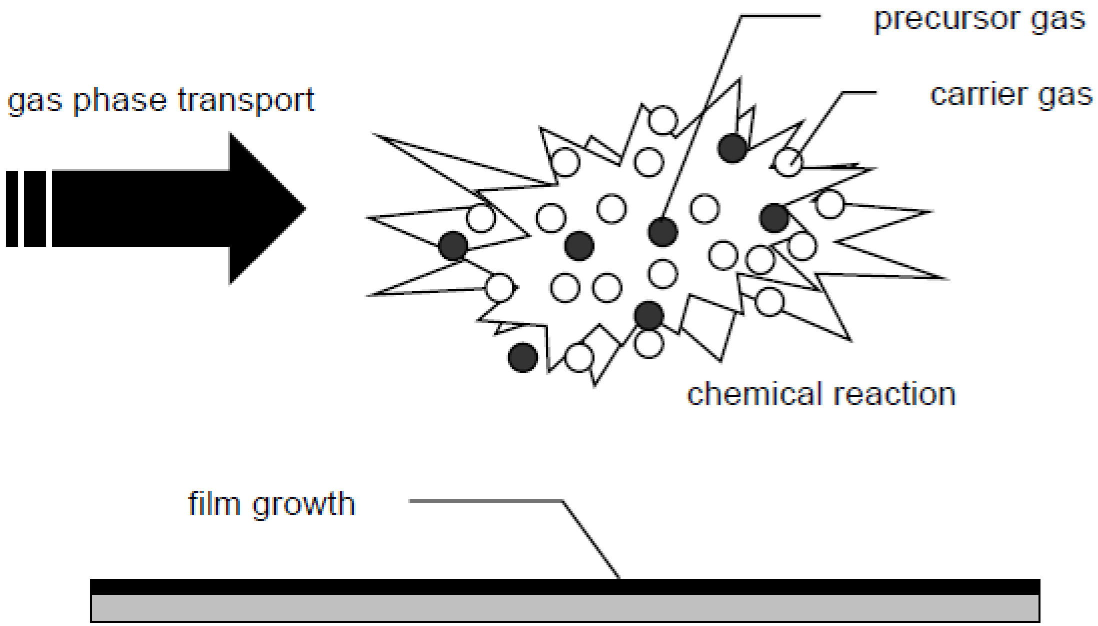
$$\vec{F} = q(\vec{E} + \vec{v} \times \vec{B})$$

Magnetron principle

Comparison of evaporation and sputtering

Evaporation	Sputtering
Limited to lighter elements and simple compounds	Virtually anything can be sputtered
Low energy ions/atoms (~0.1 eV)	High energy ions/atoms (~1-10 eV)
High purity **thin films**	Gas atoms implanted in films → lower purity
Less dense films, large **grain size**, adhesion problems	Dense films, smaller grain size, good adhesion
Requires a high-vacuum	Can use a low vacuum ~10^{-2} to 10^{-1} torr
Directional → can use for **lift-off**	Poor directionality → **good step coverage**
Components evaporate at different rates → composition of deposited film is different than source	**Components** deposited at similar rates

Chemical vapor deposition



Basic chemical vapor deposition process

Chemical Vapor Deposition (CVD)

Common way to deposit **polycrystalline** silicon thin films (often called simply “poly”

Using **silane**:

$SiH_4 \rightarrow Si +$

Using **trichlorosilane**:

$HSiCl_3 \rightarrow Si +$

Chemical vapor deposition

Silicon dioxide (SiO_2) thin films

Using **silane**:

$SiH_4 + O_2 \rightarrow$

Using **dichlorosilane** and **nitrous oxide**:

$SiCl_2H_2 + N_2O \rightarrow SiO_2$

Uses?

- *Insulator*
- *Structural layer*
- *Chemical barrier*

Silicon nitride (Si_3N_4) thin films

Using **silane**:

$SiH_4 + NH_3 \rightarrow Si_3N_4$

Using **dichlorosilane**:

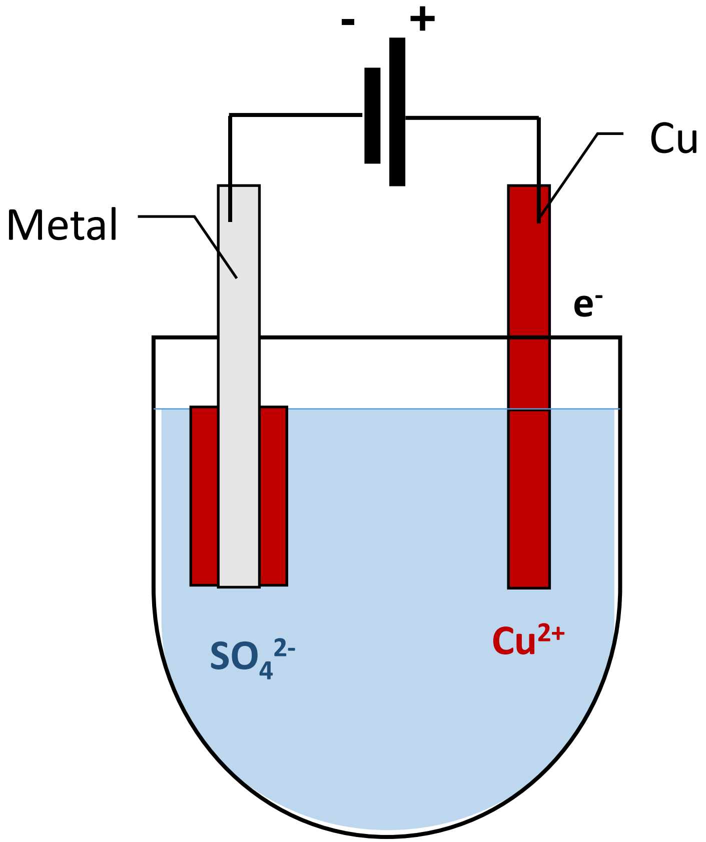
$SiCl_2H_2 + NH_3 \rightarrow Si_3N_4 +$

Comparison of PVD and CVD

PVD	CVD
• Evaporation is limited to certain materials. Sputtering has yield problems.	• Preferred method for • polysilicon layers and • silicon nitride
• Generally no hazardous byproducts	• Hazardous byproducts
• Lower temperatures	• Often requires high temperatures (~500°-850°C) → Cannot deposit on top of many metal layers
• Requires a high-vacuum	• Requires a high-vacuum (LPCVD is most common)
• **Directional** → can use for **lift-off**	• Poor directionality → **good step coverage**

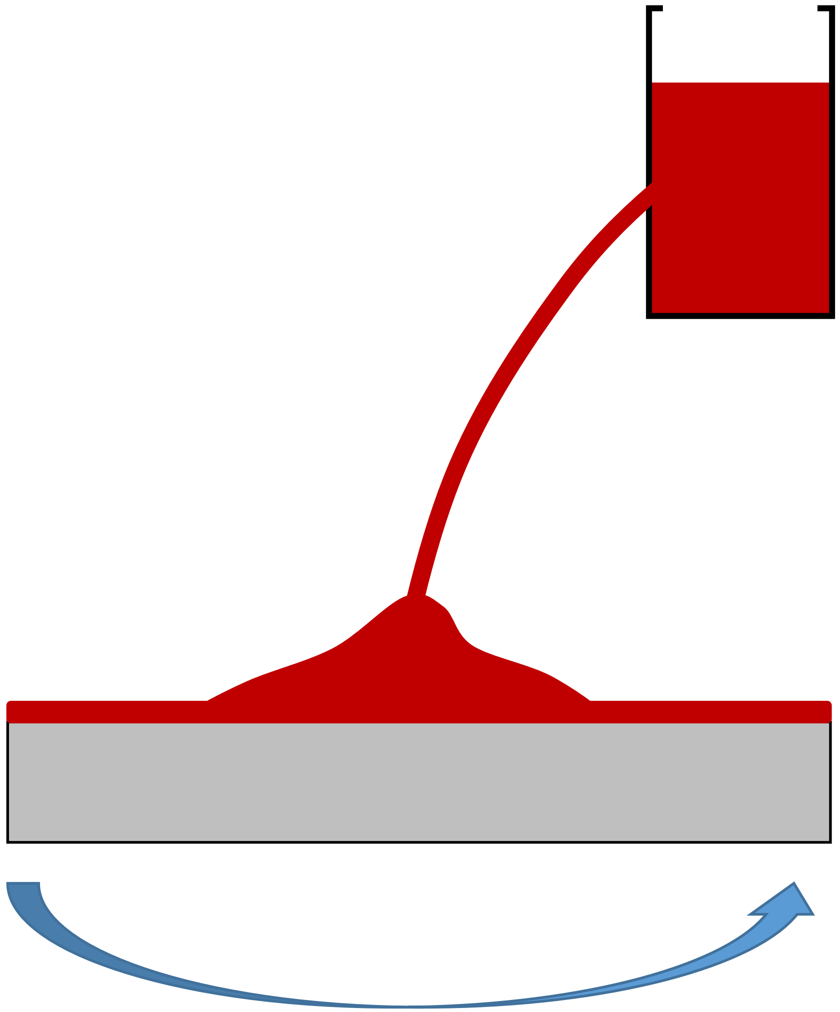
Other deposition methods

Electrodeposition (electroplating)



- Often used to deposit metals and magnetic materials
- Inexpensive and easy
- Surface quality usually worse than PVD (higher roughness)
- Uniformity can be an issue

Spin casting



Material is

- dissolved in solution,
- poured onto wafer, and
- the wafer is spun to distribute the solution across surface
- Wafer is then baked to remove the solvent, leaving behind the thin film.

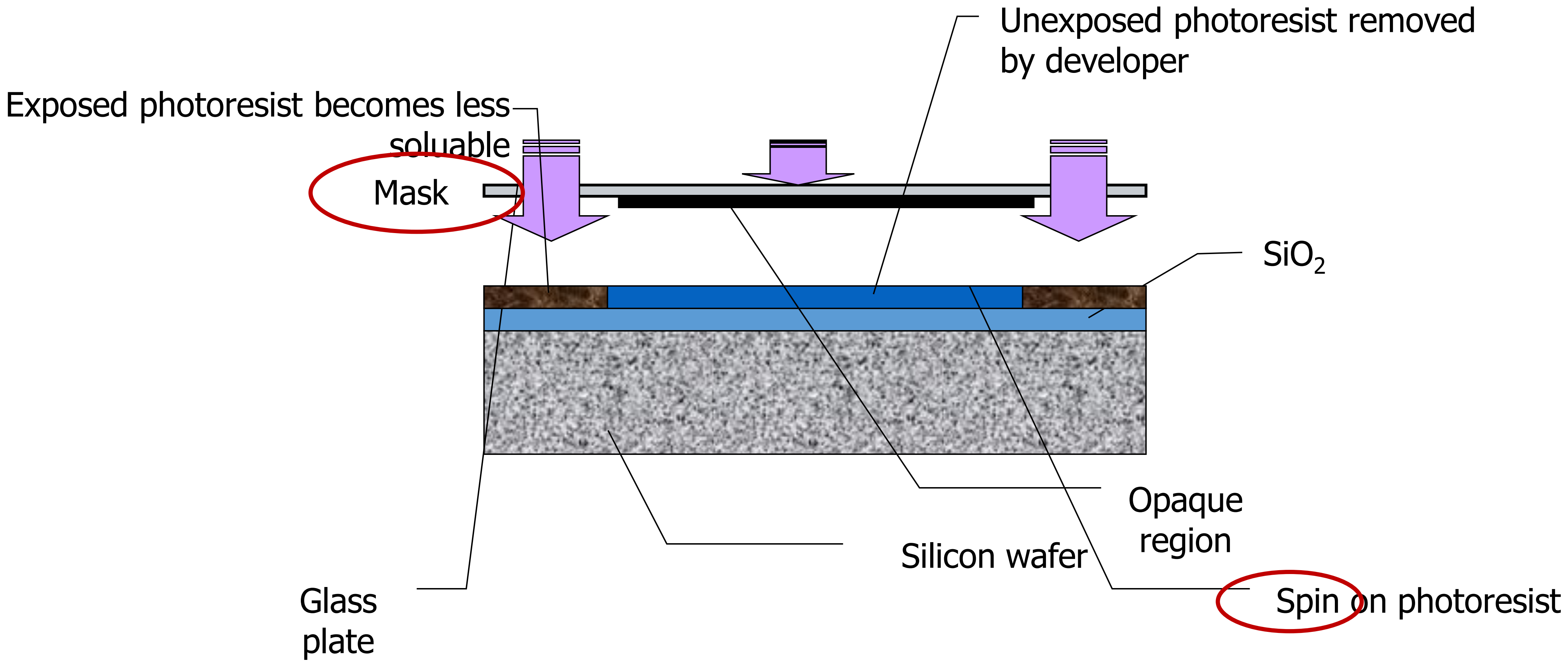
Also called simply “**spinning**”

Used for polymers, piezoelectric materials, and is the standard method of applying **photoresist**.

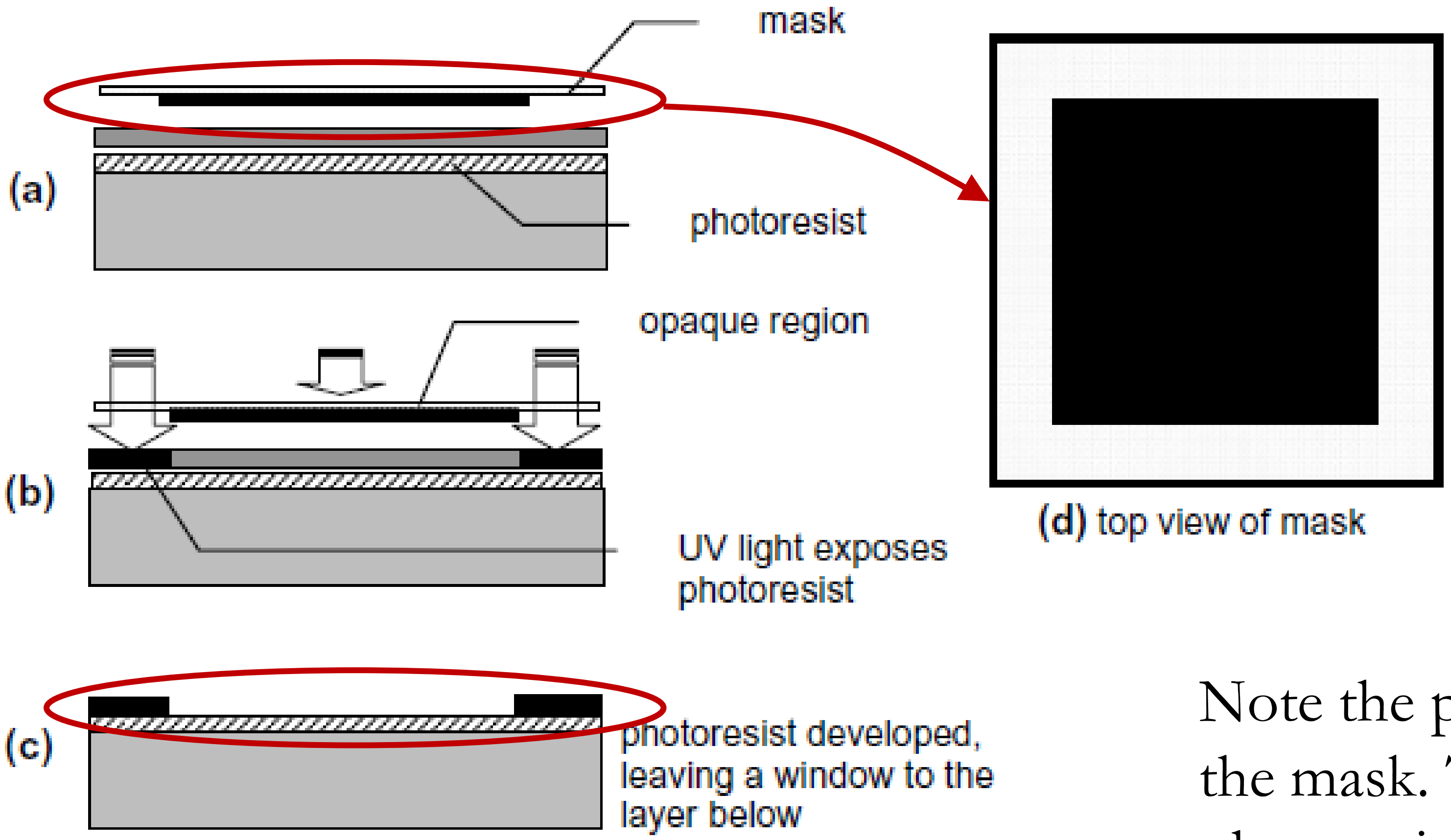
Photolithography -Step 3

- ❑ Identify the basic steps of a photolithographic process
- ❑ Describe the differences between **positive** and **negative photoresist**
- ❑ Explain why photolithography requires a clean environment
- ❑ Classify **cleanrooms** using both ISO and US FED standards
- ❑ Describe the process of a **RCA clean**
- ❑ Describe the process of applying resist via **spinning**
- ❑ Explain the need for and use of **alignment marks**

Reminder of the photolithography steps in the μ-machining process



Reminder of the photolithography steps in the µ-machining process



(d) top view of mask

Note the pattern is the opposite of that on the mask. This is true for **negative** photoresist.

Keeping it clean

Photolithography can be the “bottle neck” in terms of how small you can make a MEMS structure.

Dust particles on masks behave as extra opaque regions and transfer unwanted patterns.

→ Photolithography must be done is a very clean environment.

Clean rooms

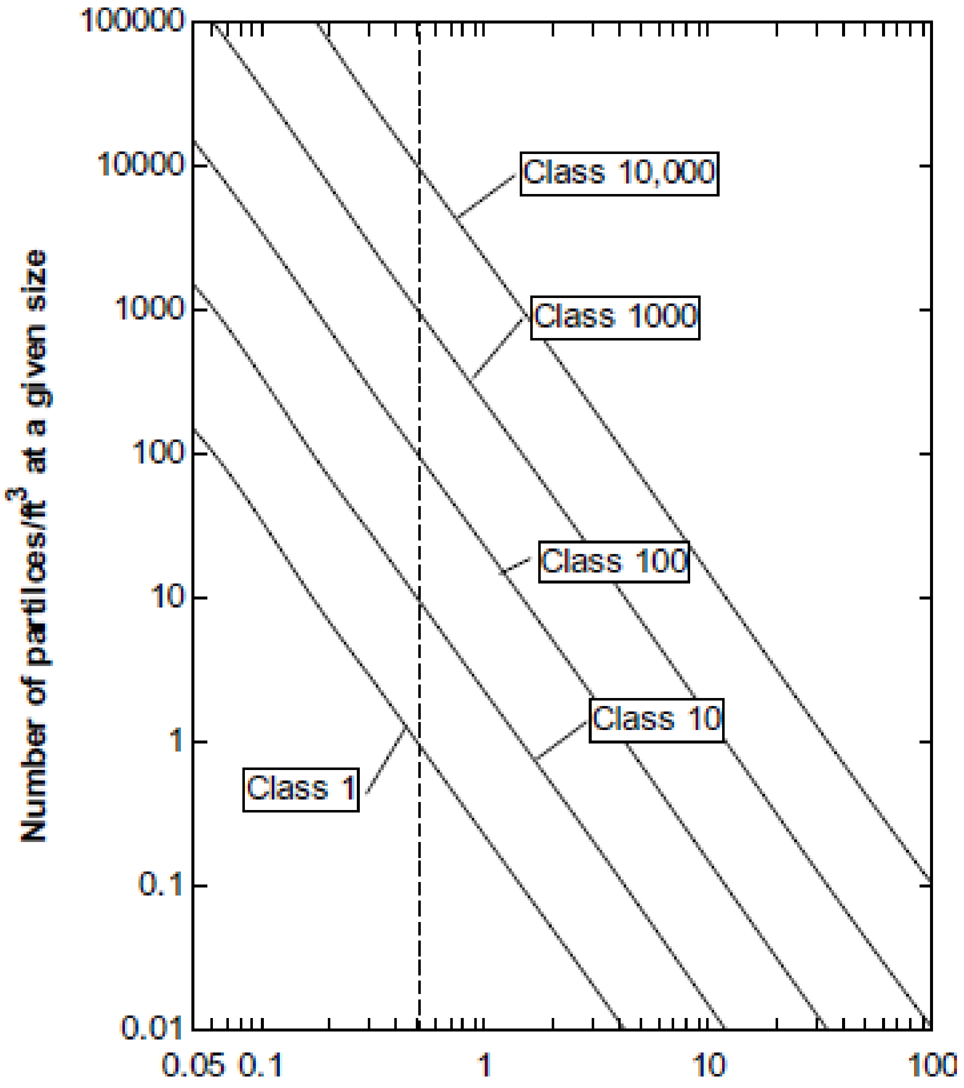
Clean rooms are classified based on how many particles of a certain size exist within a certain volume:

In the EU.

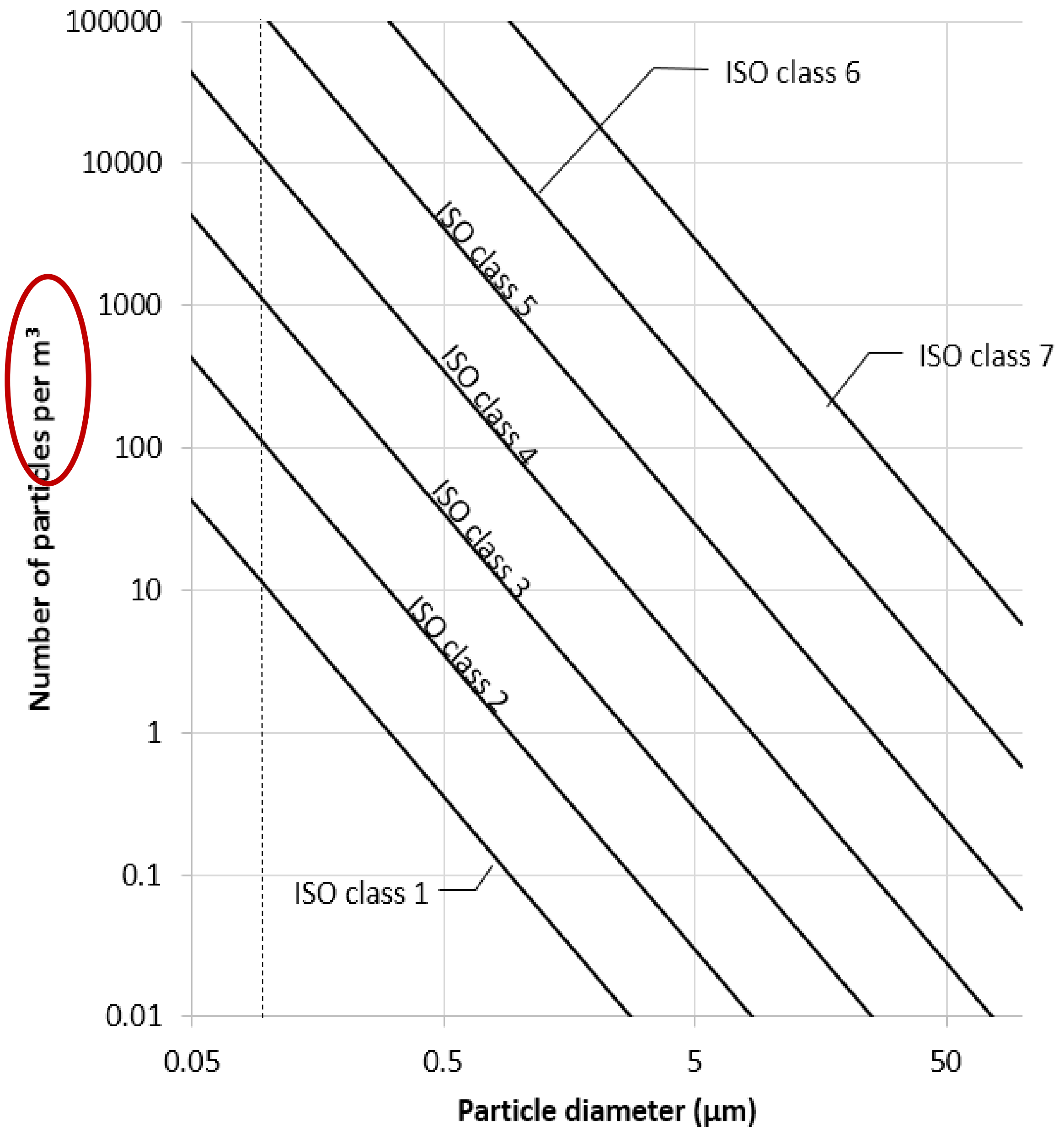
- Class 1 → less than 1 particle > 0.5 μm/ft^3
- Class 10 → less than 10 particles > 0.5 μm/ft^3
- Class 100 → less than 100 particles > 0.5 μm/ft^3
- Class 1000 → less than 1000 particles > 0.5 μm/ft^3

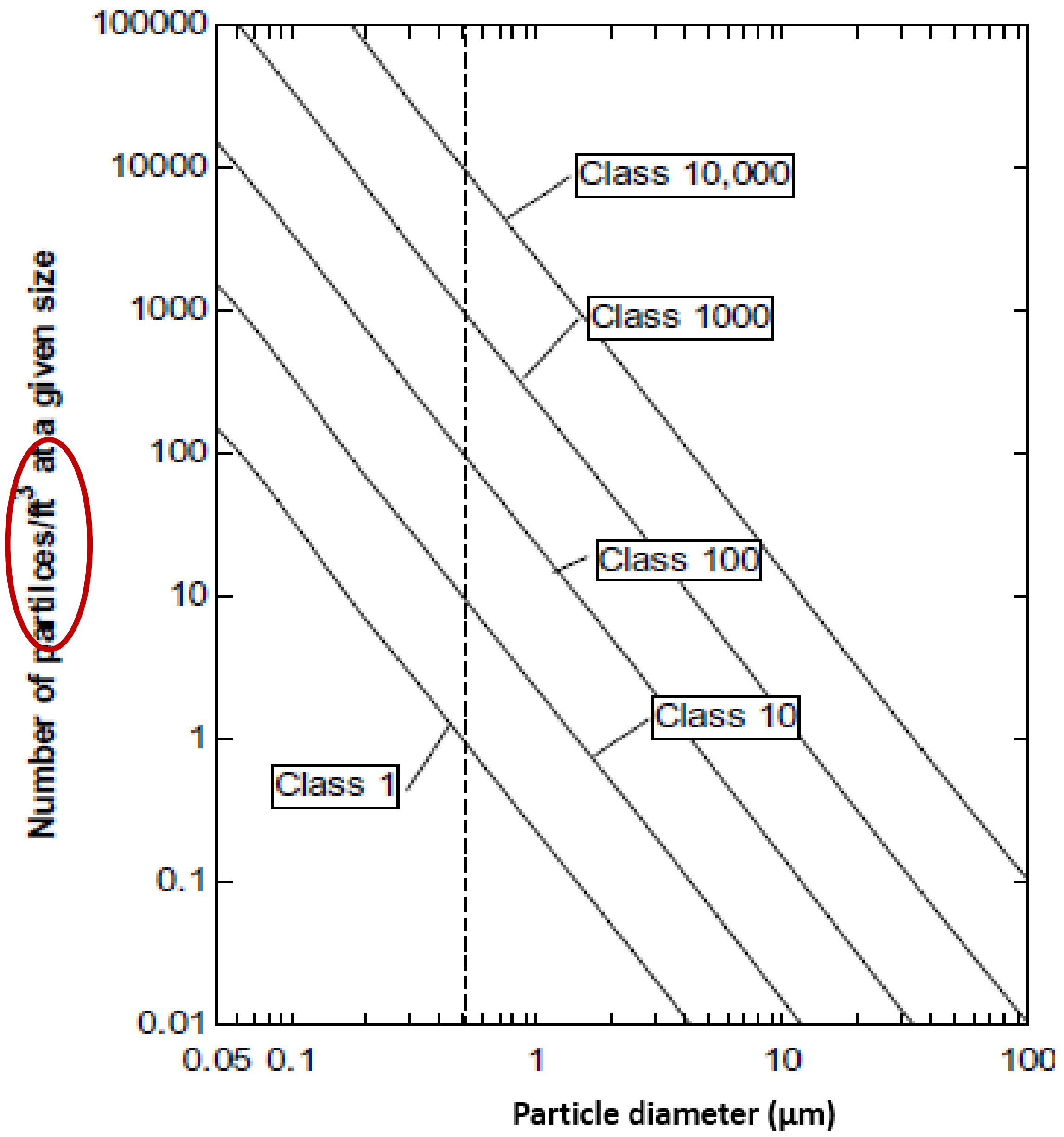
Outside the US (ISO 14644-1)

- ISO Class 1 → less than 10 particles > 0.1 μm/m^3
- ISO Class 2 → less than 100 particles > 0.1 μm/m^3
- ISO Class 3 → less than 1000 particles > 0.1 μm/m^3

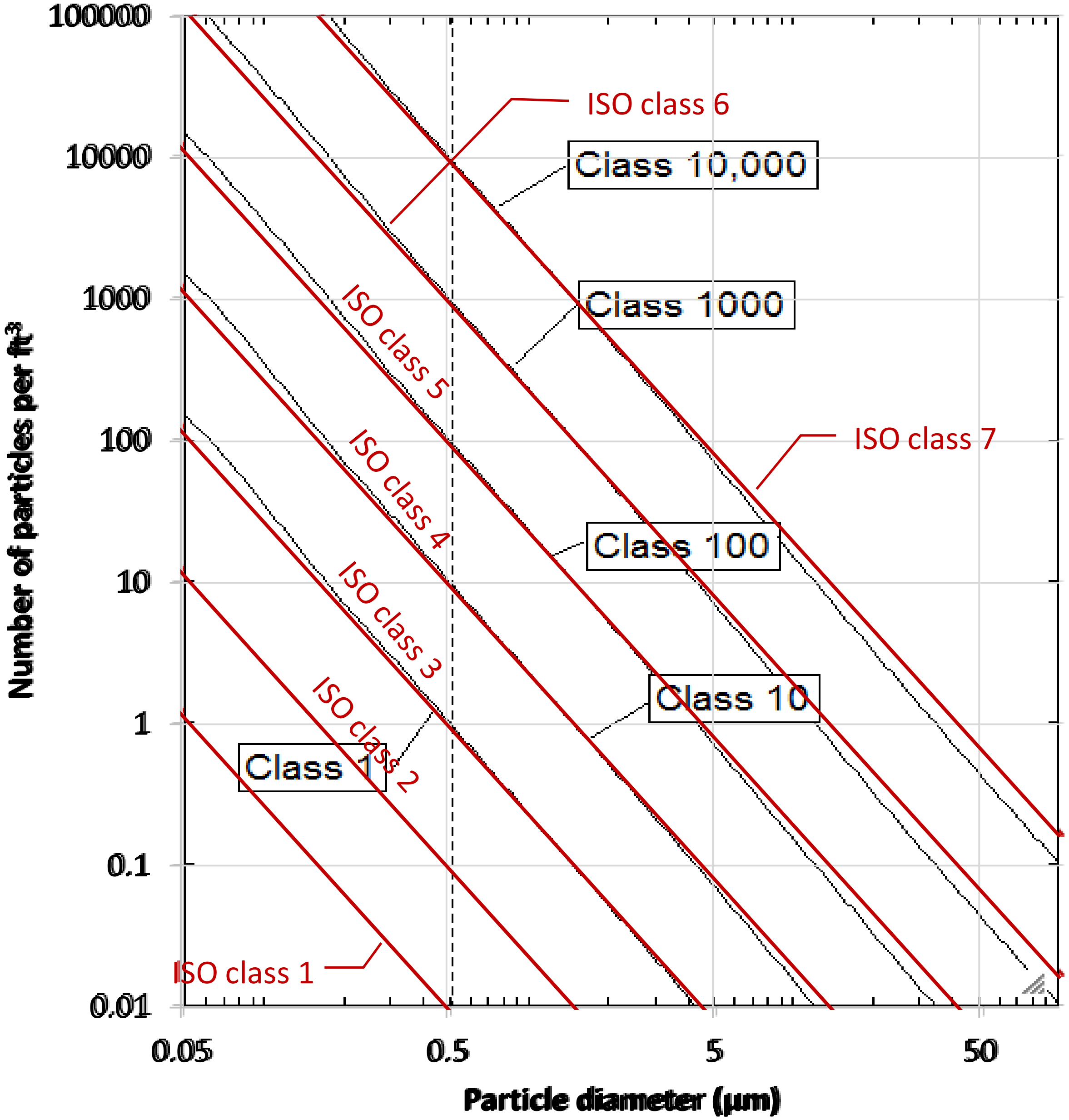


Comparison of cleanroom standards





Comparison of cleanroom standards



$$C_n = 10^N (0.1 / D)^{2.08}$$

Equivalency of cleanroom classifications

ISO 14644-1	US FED STD 209E
ISO 1	-
ISO 2	-
ISO 3	Class 1
ISO 4	Class 10
ISO 5	Class 100
ISO 6	Class 1000
ISO 7	Class 10,000

$$ISO = \log(US) + 3 \qquad US = 10^{(ISO - 3)}$$

Clean room etiquette and requirements

A typical clean room facility

- "**Bunny suits**" required (main source of airborne dust is human skin)
- Not constructed near sources of pollution
- Floors are conductive for electrostatic discharge.
- Only certain types furniture are allowed
- Specially designed paper (pens no pencils)
- No eating and drinking
- Perfume, cologne and makeup are discouraged.

Wafer cleaning

RCA clean

Developed by Werner Kern in 1965 while working at RCA Laboratories

1. 1:1:5 to 1:1:7 by volume solution of NH_4OH : H_2O_2 : H_2O is used to remove organic contaminants and heavy metals
2. HCl : H_2O_2 : H_2O in a 1:1:5 to 1:2:8 volume ratio is used to remove aluminum, magnesium, and light alkali ions

Both steps approximately 20 minutes while gently heating to 75-85°C on a hot plate

There are other cleaning techniques, such as “piranha clean”

Photoresist

Photoresist is the “stuff” of photolithography

- Often called “resist”
- Three (3) components:
  1. a base resin, which is a polymer: gives the resist structure
  2. photoactive compound (PAC): The light-sensitive component
  3. solvent.
- Comes in two varieties
  1. Positive resist
  2. Negative resist

Usually sensitive to a narrow band of ultraviolet (UV) light

Positive versus negative resist

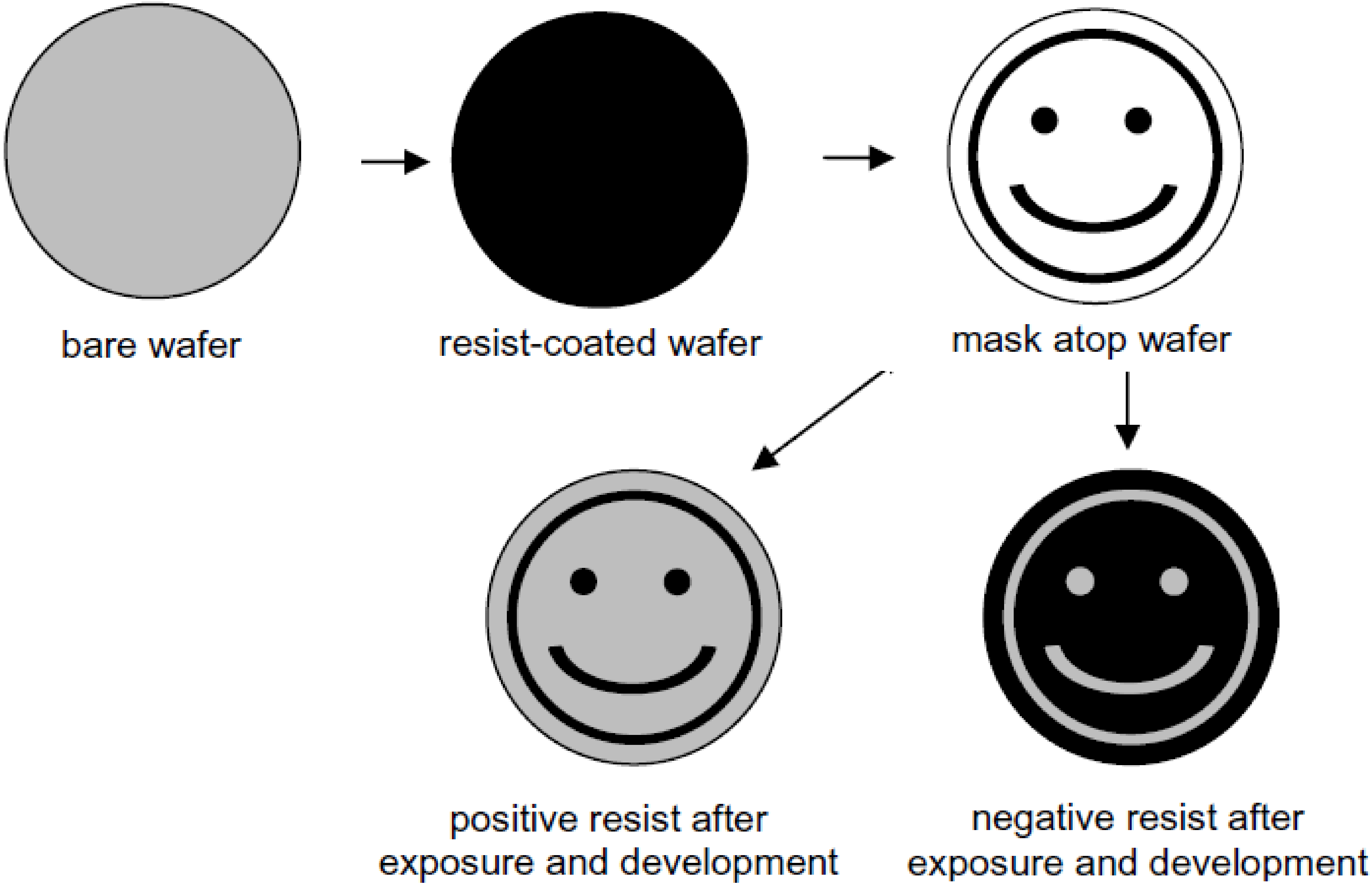
Positive resist

- Exposure degrades the PAC
- Becomes more soluble to the developer after exposure
- Unexposed regions of the resist are left behind after development
- Developed resist pattern is identical to the mask pattern.
- Alkalis such as NaOH or KOH used as developers
- Very sensitive to UV light with wavelength of 365 nm, called the **I-line** of the mercury spectrum

Negative resist

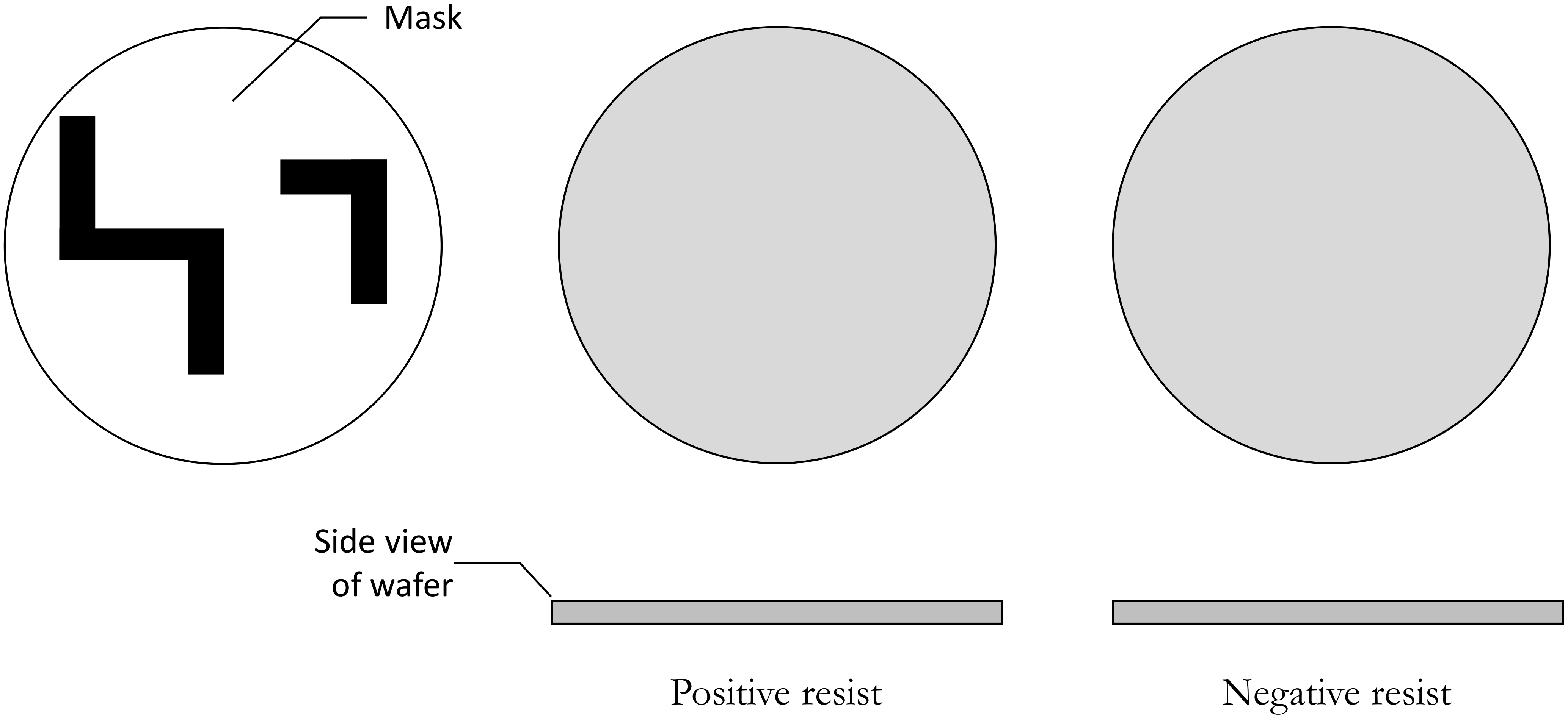
- Exposure increases MW of resist or creates new insoluble products
- Becomes less soluble to the developer after exposure
- Unexposed regions of the resist are removed after development
- Developed resist pattern is the opposite of the mask pattern.
- Organic solvents such as benzene used as developers
- Very sensitive to UV light with wavelength of 405 nm, called the **H-line** of the mercury spectrum
- ~ 10 times more sensitive than positive resist

Positive versus negative resist

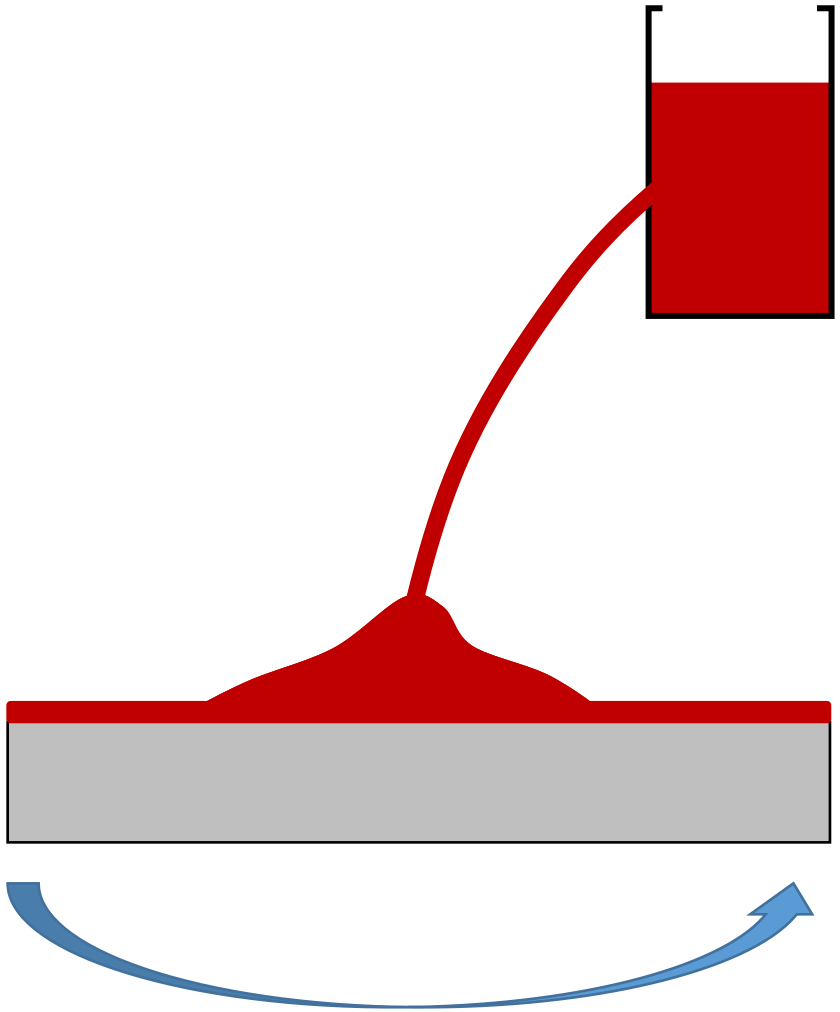


Quiz

The mask shown in the figure is used to transfer a pattern to a silicon wafer. Sketch the resulting pattern on the wafer after exposure and development for both positive and negative resist.. Also sketch the profile from the side of the wafer.



Applying resist

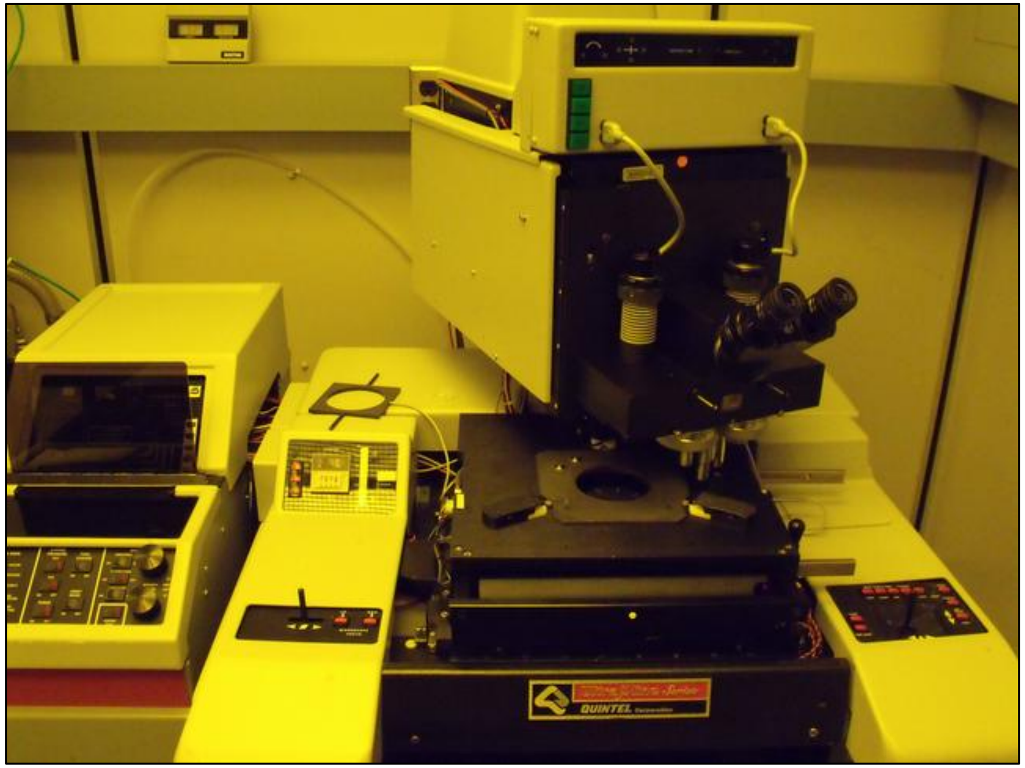


Three steps

1. A **pre-bake** to reduce water (water can the reduce adhesion of resist)
2. Spin on the resist
    - Pour it onto wafer
    - Spin wafer to distribute the solution across surface
3. A post-bake to remove the solvent

Photoresist can also be sprayed (which may or may not get around uniformity issues)

Exposure and pattern transfer



A typical contact aligner

Development and post-treatment

Positive resist

- Exposure degrades the PAC
- Becomes more soluble to the developer after exposure
- Unexposed regions of the resist are left behind after development
- Developed resist pattern is identical to the mask pattern.
- Alkalis such as NaOH or KOH used as developers

Negative resist

- Exposure increases MW of resist or creates new insoluble products
- Becomes less soluble to the developer after exposure
- Unexposed regions of the resist are removed after development
- Developed resist pattern is the opposite of the mask pattern.
- Organic solvents such as benzene used as developers

Development and post-treatment

After exposure, a mild oxygen **plasma** can be used to remove leftover exposed/unexposed resist.

Plasma ashing

A **post-bake** follows, hardening resist even more.

After the resist has done what it needs to do (act as a mask for doping, or for the etching of the layer below, e.g.,) resist needs to be removed completely → **stripping**

Positive resist

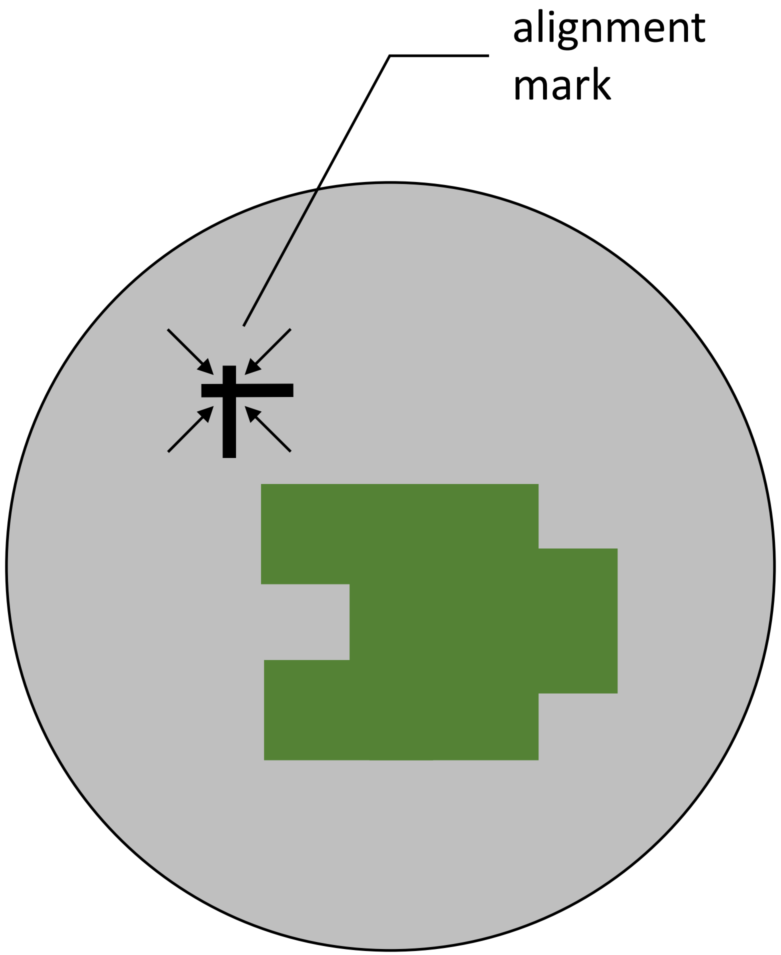
- Wet stripping usually used
- Chemical solvent such as acetone or methylethylketone (C_4H_8O)
- Often requires $T \sim 80°C$
- Can ignite with O_2!
- Safety important

Negative resist

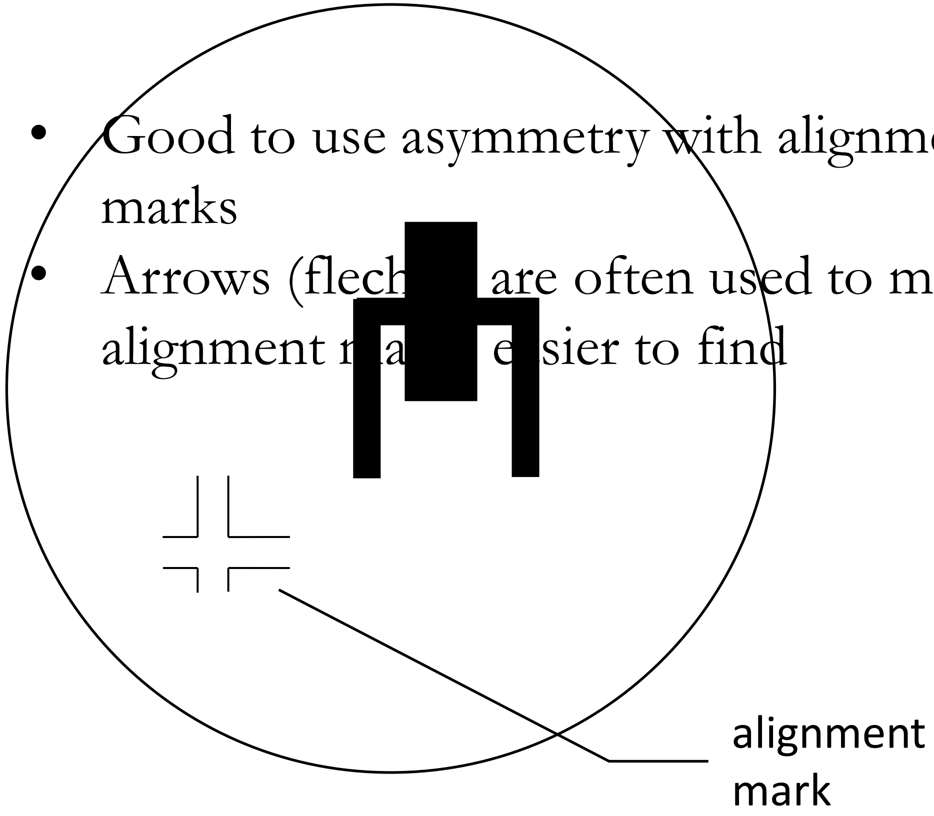
- Harder to remove
- Use of acids and/or chlorinated hydrocarbons; e.g., H_2SO_4 and H_2O_2 at 150°C ("piranha" clean)
- Sometimes a **plasma ash** required.

Mask alignment

Mask alignment also called registration



Processed wafer



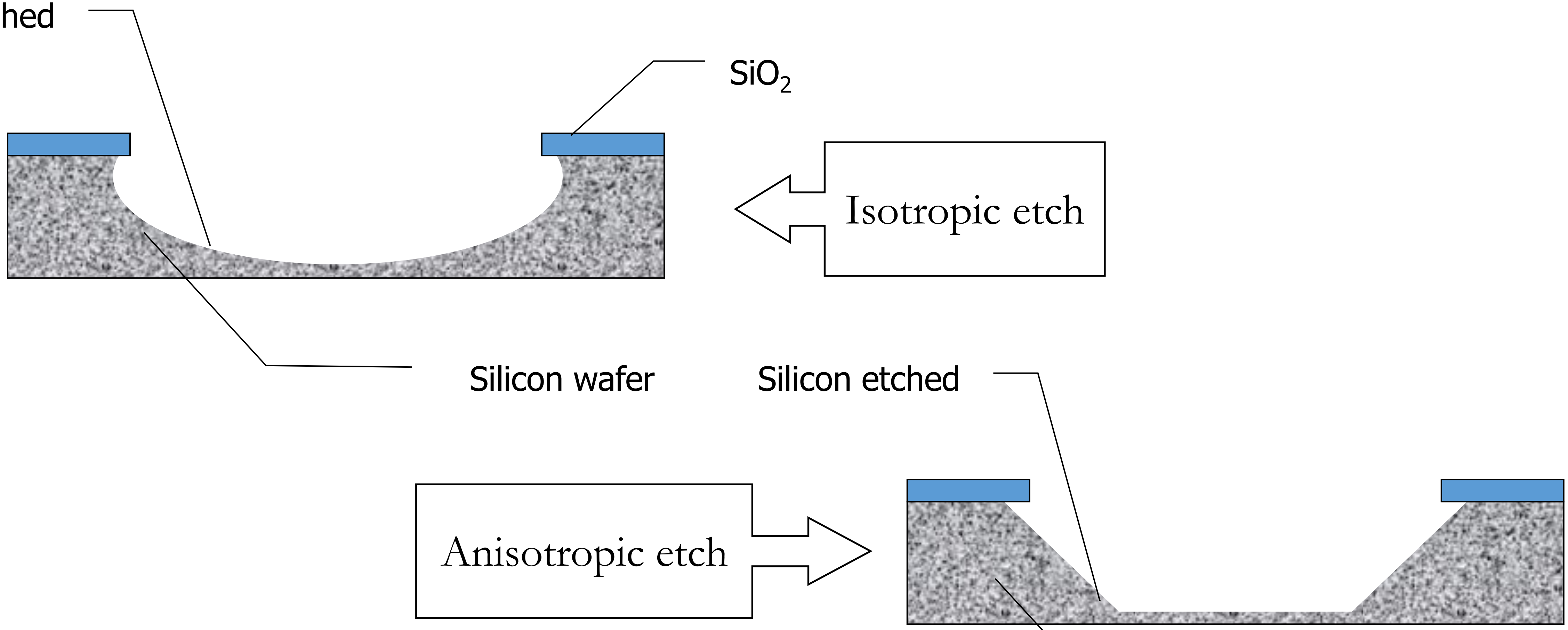
Mask

- Good to use asymmetry with alignment marks
- Arrows (flech are often used to make alignment ma easier to find

Bulk micromachining- Step 4

- ☐ Explain the differences between **isotropic** and **anisotropic etching**
- ☐ Explain the differences between **wet** and **dry etching** techniques
- ☐ Identify several common wet etchants and explain what they are commonly used for
- ☐ Discern the resulting shapes of trenches (pits) resulting from the anisotropic etching of Si for different mask and wafer combinations
- ☐ List and explain the most common **etch stop** techniques
- ☐ List and describe the most common dry etching techniques
- ☐ Perform basic calculations for wet etching processes

Bulk micromachining



Silicon etched

SiO_2

Isotropic etch

Silicon wafer

Silicon etched

Anisotropic etch

Silicon wafer

Etching

Etching: Chemical reaction resulting in the removal of material

Wet etching: etchants in liquid form

Dry etching: etchants contained is gas or **plasma**

ionized gas

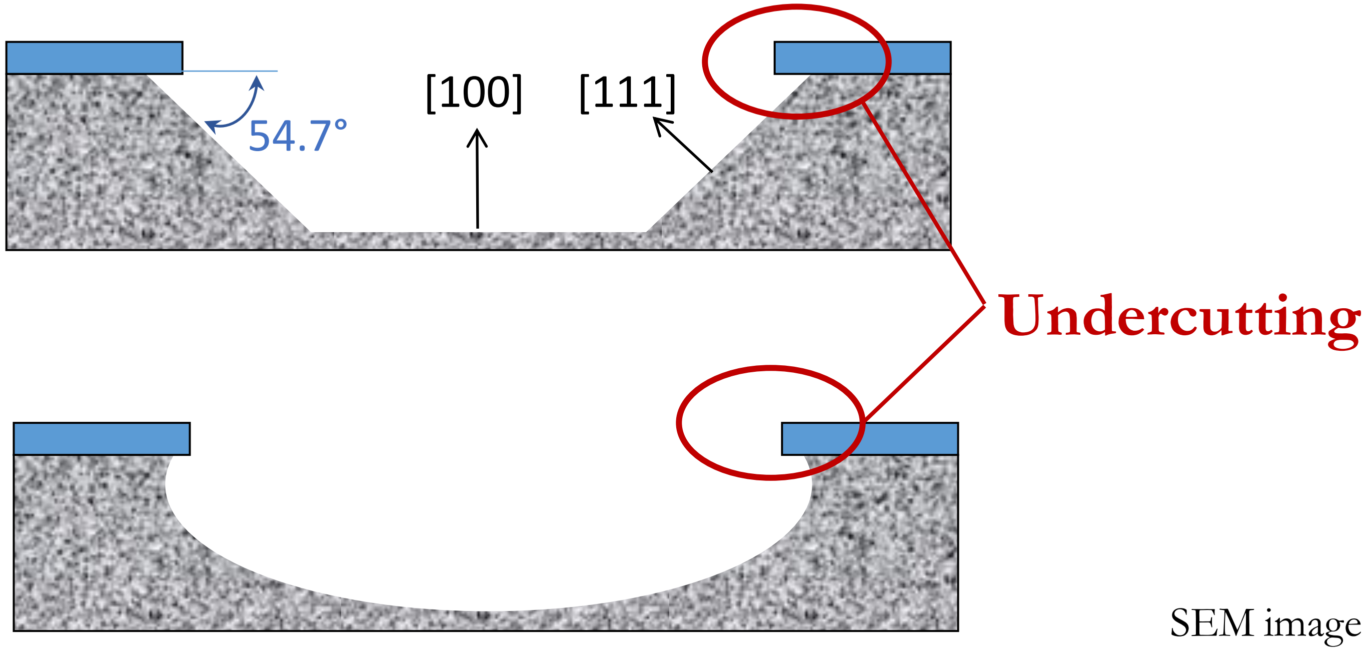
Etch rate: material removed per time (μm/min)

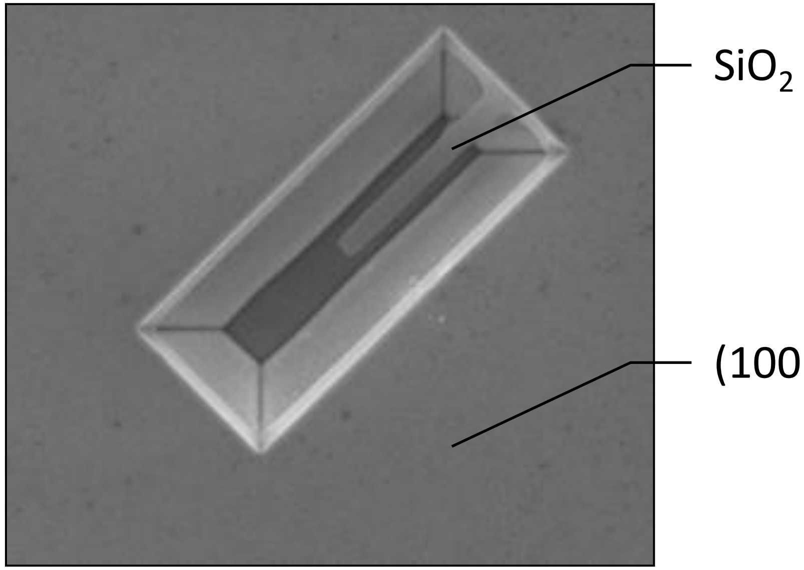
Selectivity and undercutting

Selectivity:

etch rate of one material compared to another

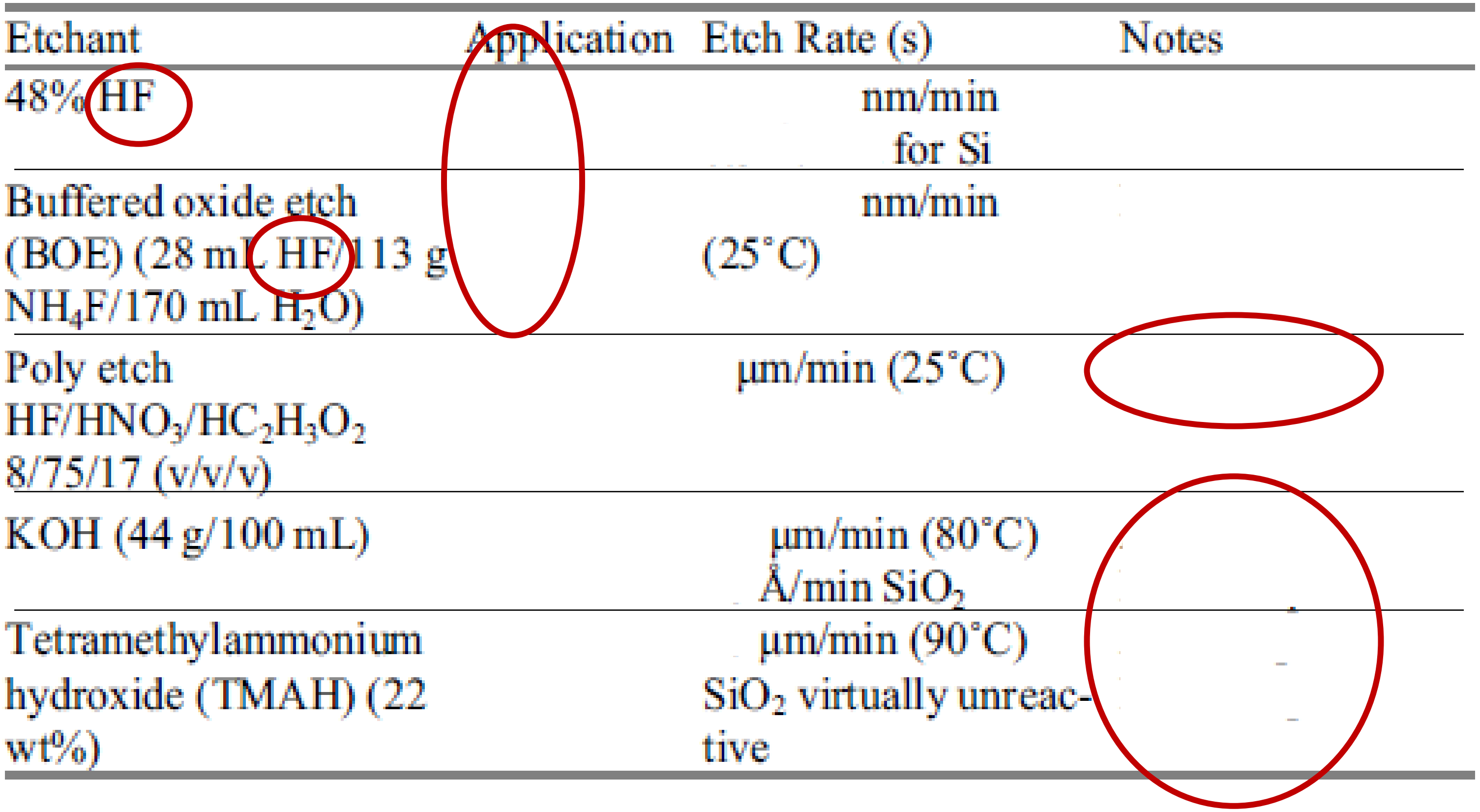
etch rate of one crystalline direction compared to another





SEM image of a SiO_2 cantilever formed by undercutting (S. Mohana Sundaram and A. Ghosh, Department of Physics, Indian Institute of Science, Bangalore)

Application and properties of different wet etchants



Etchant	Application	Etch Rate (s)	Notes
48% HF		nm/min for Si	
Buffered oxide etch (BOE) (28 mL HF/113 g NH_4F/170 mL H_2O)		nm/min (25°C)	
Poly etch $HF/HNO_3/HC_2H_3O_2$ 8/75/17 (v/v/v)		µm/min (25°C)	
KOH (44 g/100 mL)		µm/min (80°C) Å/min SiO_2	
Tetramethylammonium hydroxide (TMAH) (22 wt%)		µm/min (90°C) SiO_2 virtually unreactive	

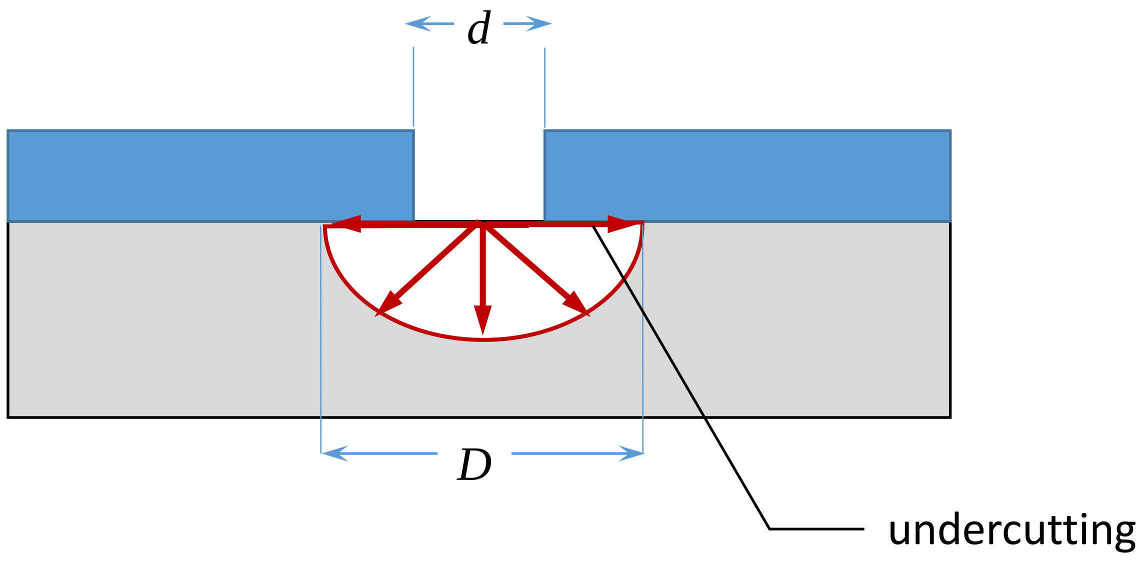
High HF tends to etch SiO_2

Acidic etchants tend to etch Si isotropically

Basic etchants tend to etch Si anisotropically

Depend on concentration and temperature

Isotropic etching



Estimate of etch depth

$$\text{depth} \approx (D\text{-}d)/2$$

- Etch rate is the same in all directions
- Typically acidic
- Room temperature
- Isotropy is due to the fast chemical reactions → Reaction or diffusion limited?
- X μm/min to XX μm/min

Isotropic etching

HNA: $HF/HNO_3/HC_2H_3O_2$

- Used in isotropic etching of silicon
- Also called **poly etch**

$$HNO_3\ (aq) + Si(s) + 6HF\ (aq) \rightarrow H_2SiF_6\ (aq) + HNO_2\ (aq) + H_2O\ (l) + H_2\ (g)$$

The etching process actually occurs in several steps.

First step, nitric acid oxidizes the silicon

$$HNO_3\ (aq) + H_2O\ (l) + Si\ (s) \rightarrow SiO_2\ (s) + HNO_2\ (aq) + H_2\ (g)$$

In the second step, the newly formed silicon dioxide is etched by the hydrofluoric acid.

$$SiO_2\ (s) + 6HF\ (aq) \rightarrow H_2SiF_6\ (aq) + 2\ H_2O\ (l)$$

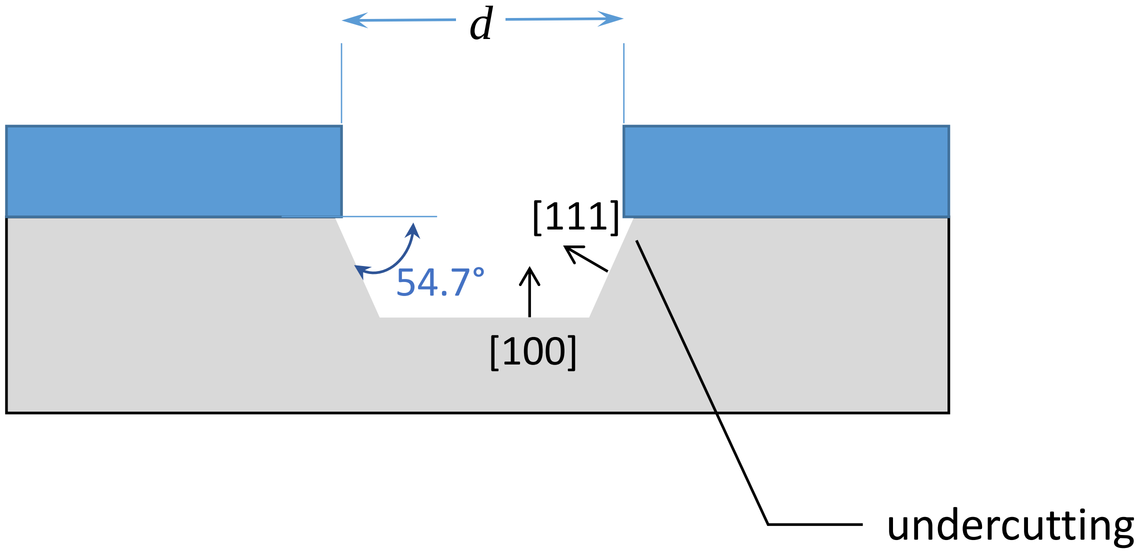
Isotropic etching

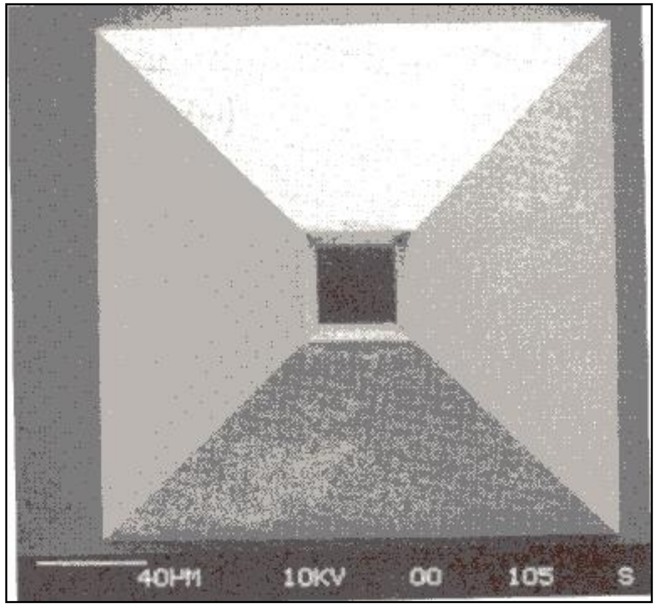
BOE (Buffered Oxide Etch): $HF/NH_4F/H_2O$

- Used in isotropic etching of silicon dioxide and glass
- Basically proceeds from the second step of etching Si:

$$SiO_2\,(s) + 6HF\,(aq) \rightarrow H_2SiF_6\,(aq) + 2\,H_2O\,(l)$$

Anisotropic etching

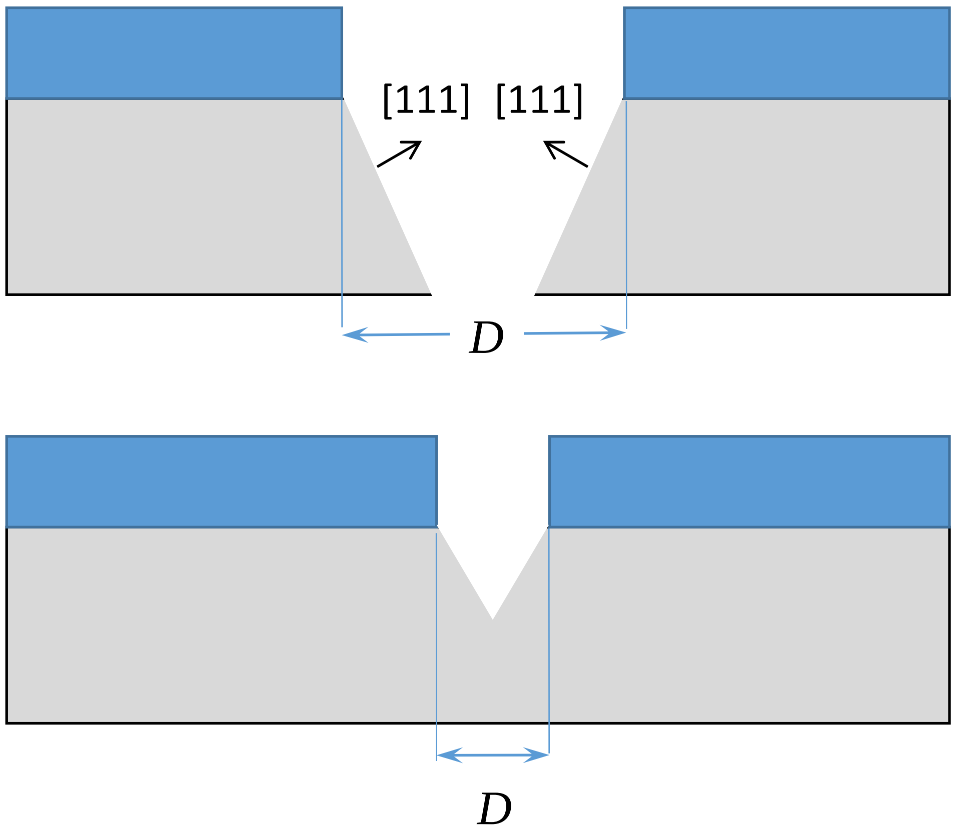


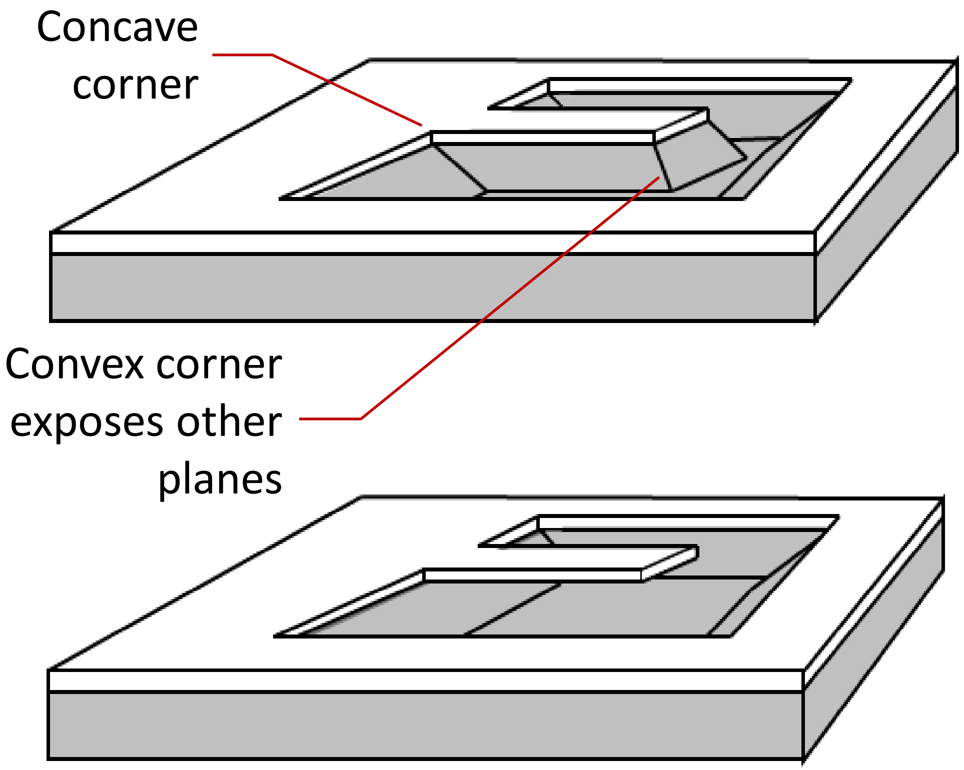


- Etch rate is different for different crystal plane directions
- Typically basic etchants
- Elevated temperatures (70-120°C)
- Different theories propose for anisotropy
- Slower etch rates, ~ 1 μm/min → Reaction or diffusion limited?

- Etch depths depend on geometry
- Undercutting also depends on geometry

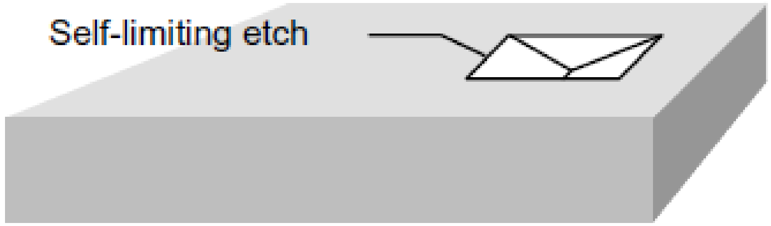
Self-limiting etch and undercutting





Resulting undercutting can be used to create suspended structures

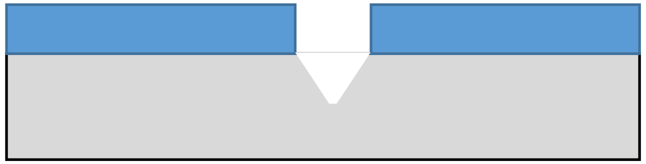
- Intersection of {111} planes can cause **self-limiting** etch.
- Only works with concave corners



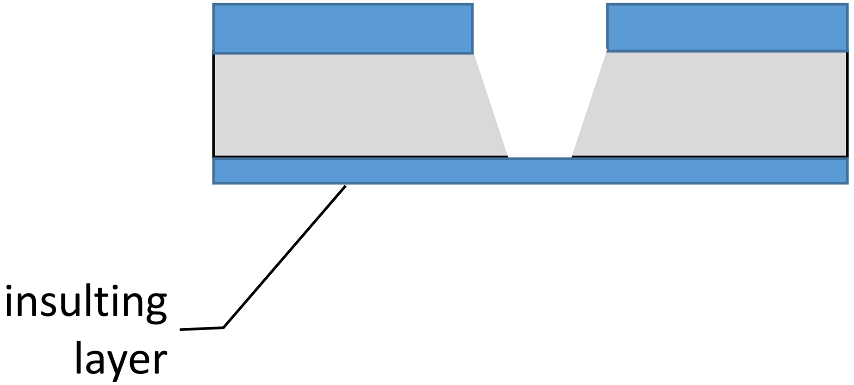
Etch stop

Etch stop: Technique to actively stop the etching process

Self-limiting etch

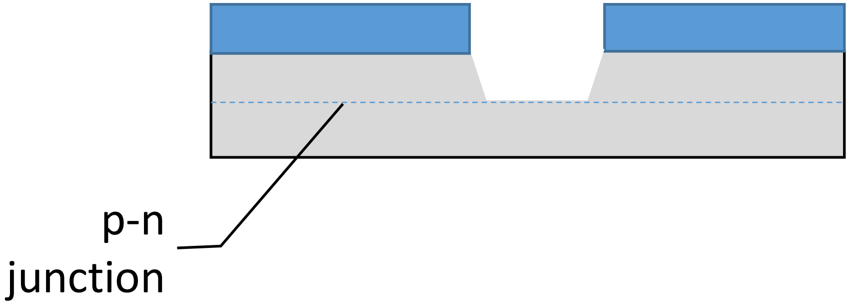


Insulator etch stop



Timed etch

Etch stop via doping

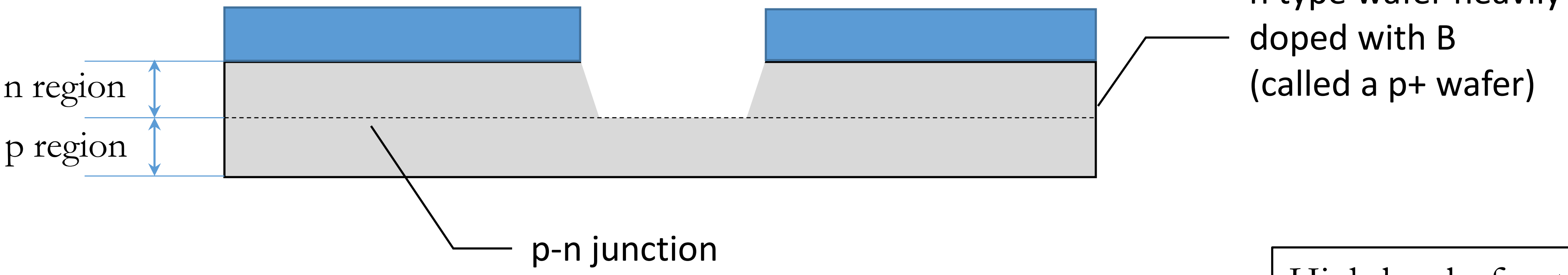


Etch stop via doping

Boron etch stop

$Si + 2\cancel{OH^- \rightarrow SiOH_2^{++}} + 4\ e^-$ (oxidation step)

$SiOH_2^{++} + 4\ e^- + 4\ H_2O \rightarrow Si(OH)_6^{--} + 2\ H_2$ (reduction step)



p region Si deficient in e^-

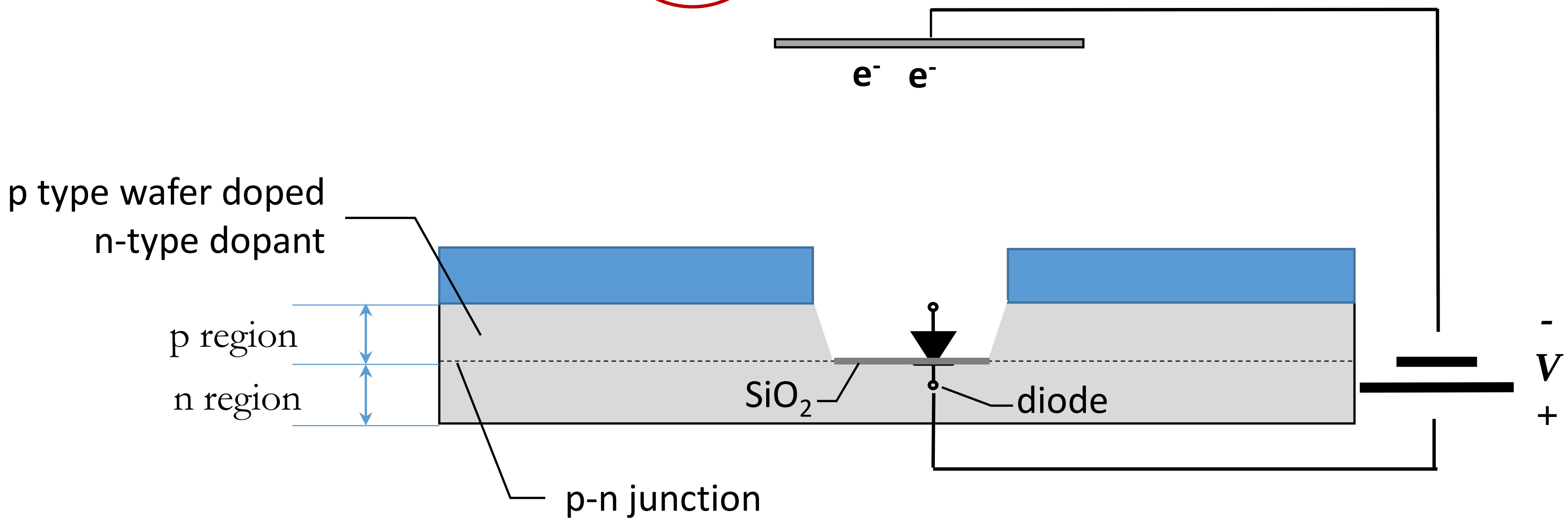
High level of p-type doping is not compatible with CMOS standards for integrated circuit fabrication

Etch stop via doping

Electrochemical etch stop (ECE)

$$\mathrm{Si} + 2\mathrm{OH}^- \rightarrow \mathrm{SiOH}_2^{++} + 4\,e^-$$ (oxidation step)

$$\mathrm{SiOH}_2^{++} \cancel{+ 4\,e^- +} 4\,\mathrm{H}_2\mathrm{O} \rightarrow \mathrm{Si(OH)}_6^{--} + 2\,\mathrm{H}_2$$ (reduction step)



"Reverse bias" voltage applied to p-n junction keeps current from flowing

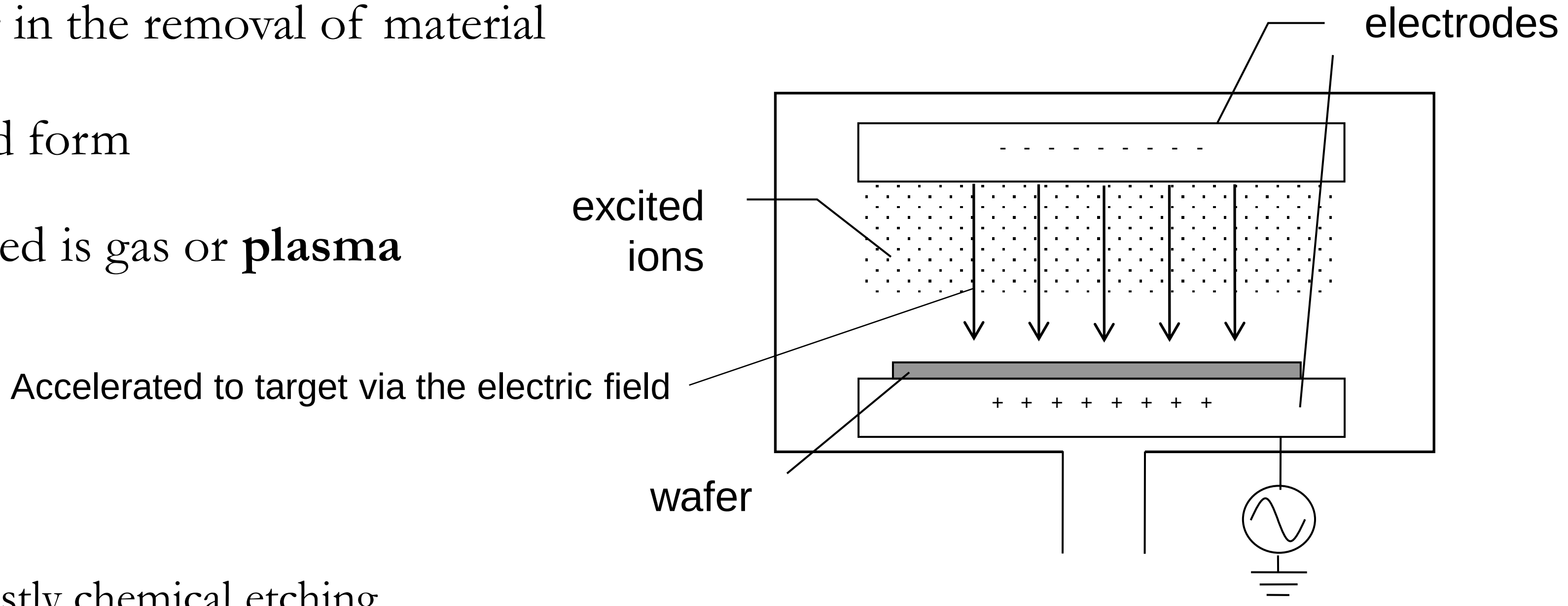
Very light doping compared to boron etch stop. OK with CMOS standards for integrated circuit fabrication.

Dry etching

Etching: Chemical reaction resulting in the removal of material

Wet etching: etchants in liquid form

Dry etching: etchants contained is gas or **plasma**



Plasma etching: mostly chemical etching

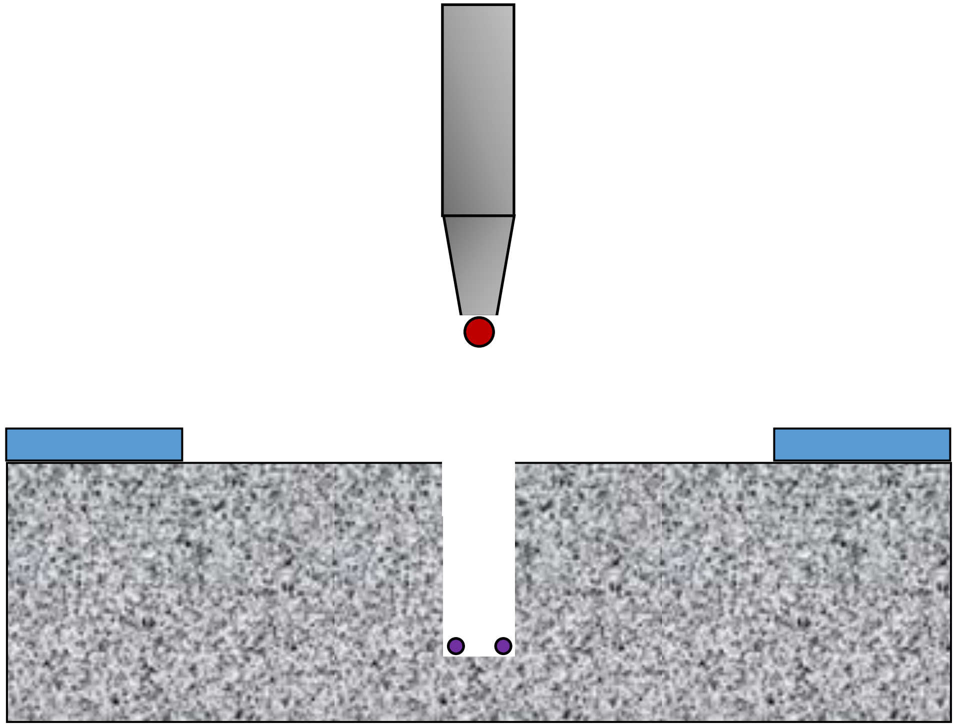
Reactive ion etching (RIE):

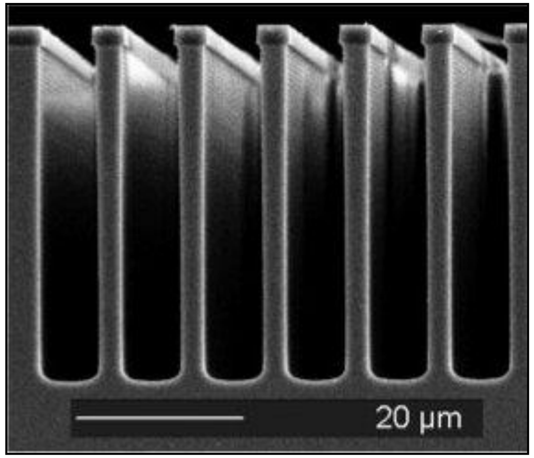
In addition to the chemical etching, accelerated ions also physically etch the surface

Chemically reactive gas formed by collision of

- molecules of reactive gas with
- energetic electrons
- Excited/ignited be RF (radio frequency) electric field ~ 10-15 MHz

Reactive ion etching





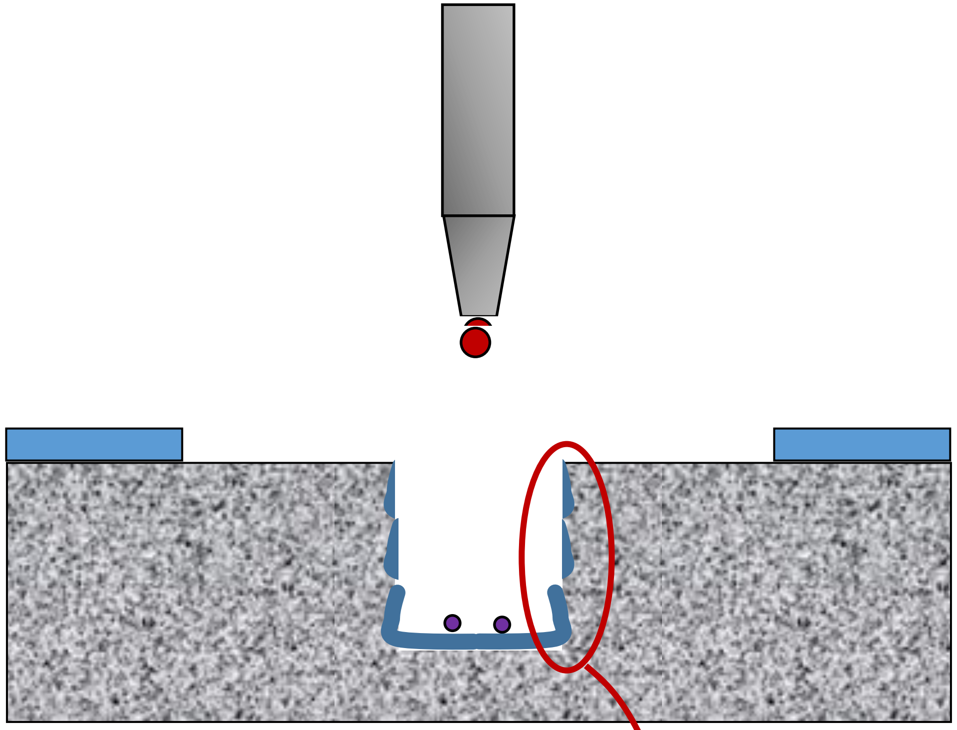
(Intellisense Corporation)

Plasma hits surface with large energy

- In addition to the chemical reaction, there is physical etching (Parece tirar piedras en la arena)
- Can be very directional—can create tall, skinny channels

If there is no chemical reaction at all, the technique is called **ion milling.**

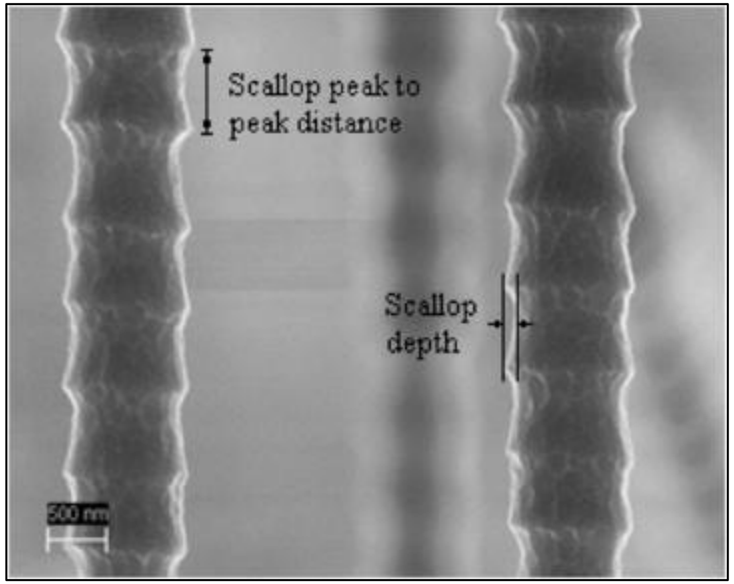
Deep reactive ion etching (DRIE)



Bosch process

- 1st, reactive ion etching step takes place
- 2nd, fluorocarbon polymer deposited to protect sidewalls

“Scalloping”



Kane Miller, Mingxiao Li, Kevin M Walsh and Xiao-An Fu, **The effects of DRIE operational parameters on vertically aligned micropillar arrays**, *Journal of Micromechanics and Microengineering*, **23** (3)

Wet etching

- 40 years of experience and data in the semiconductor industry
- Ability to remove surface contaminants
- Very high **selectivity's**
- Usually **isotropic** → always involve **undercutting**

Dry etching

- Better **resolution** than wet etching
- More **directionality** (High **aspect ratios**)
- Lower **selectivity's**
- No **undercutting**

Quiz

Wet etching problems

1. A pattern is etched into a <100> Si wafer as described below. Answer the questions that follow.

   A 300 nm thick layer of oxide is grown on the surface of the Si wafer. Photoresist is applied to the oxide surface, and patterned using standard photolithographic techniques. The pattern is etched into the oxide. The exposed Si is etched anisotropically to achieve the desired feature.

   a. Should the photoresist be removed before the Si etching step? Yes.
   b. What etchant will you use for the oxide? →HF
   c. What wet etchant will you use for the Si? → TMAH, KOH

2. You are asked to make a V-shaped grooves 60 μm deep in an oxidized <100> silicon wafer using TMAH etching

   a. How wide must the opening in the oxide mask be in order to achieve this result?

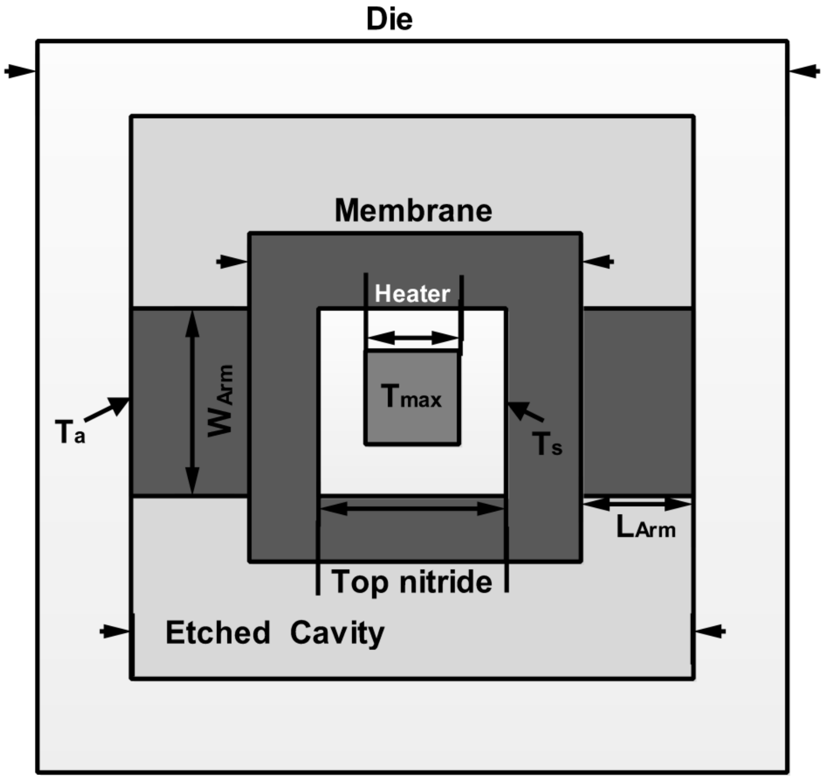
The governing equation is,

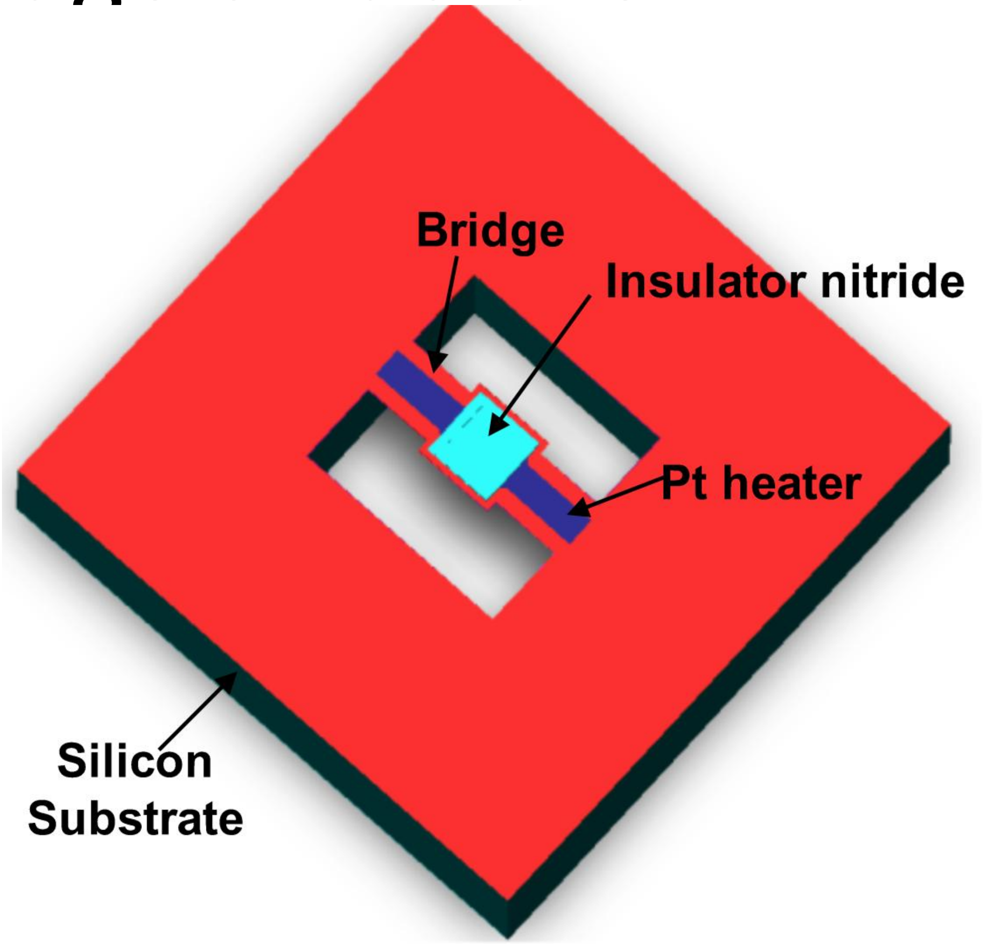
$$\underbrace{\rho c_p \frac{dT}{dt}}_{\textbf{Heat Stored}} = \underbrace{\nabla\cdot(K_{eff}\nabla T + K_{air}\nabla T - q_h - q_r)}_{\textbf{Heat Loss}} + \underbrace{\frac{P}{V}}_{\textbf{Supply}}$$

Analytical Modeling

- Fitting cat into a finite box
  - Simplify
  - Saves time
  - Quick first order optimization
- Assumption → case limited
  - Conduction
  - Convection
  - Radiation
  - Steady state
  - Directional temperature gradient

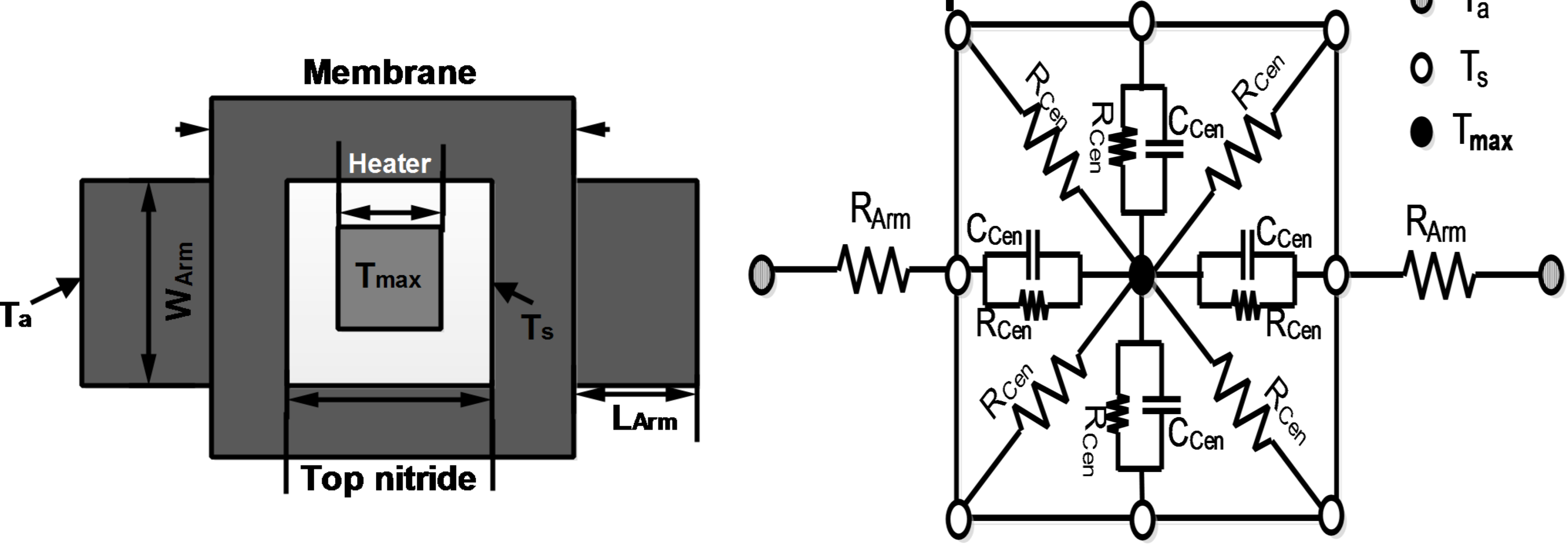
Case # - Bridge Structure





(a) Top view of a die consisting of bridge membrane (dark gray), active area (gray), etched cavity (light gray) and insulation nitride (white). (b) FEM Simulated Structure

Conversion to Lumped model



(a)

(b)

(a) Top view of bridge membrane (dark gray), active area (gray), etched cavity (light gray) and insulation nitride (white). (b) Lumped element model of the bridge membrane, Tmax is the temperature at the center of membrane, Ts and Ta are the temperatures at the edges of top nitride and ambient temperature respectively

Model

- The heat conduction equation can be written as

$$C_{tot}\frac{dT}{dt} = P_{app} - \frac{\Delta T}{R_{tot}} (1)$$

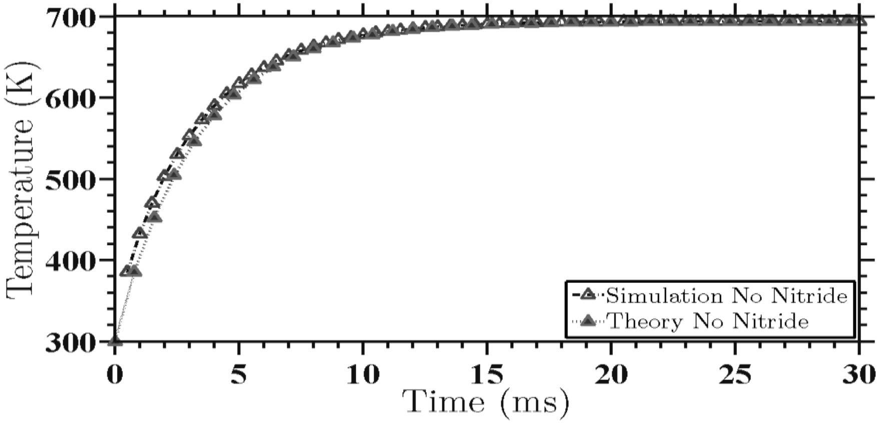
$$T(t) = T_a + P_{app}R_{tot}\left(1 - e^{\frac{-t}{R_{tot}C_{tot}}}\right)(2)$$

$$\mathrm{R}_{\mathrm{tot}} = 8\mathrm{R}_{\mathrm{Cen}} + 2\mathrm{R}_{\mathrm{Arm}} (3)$$

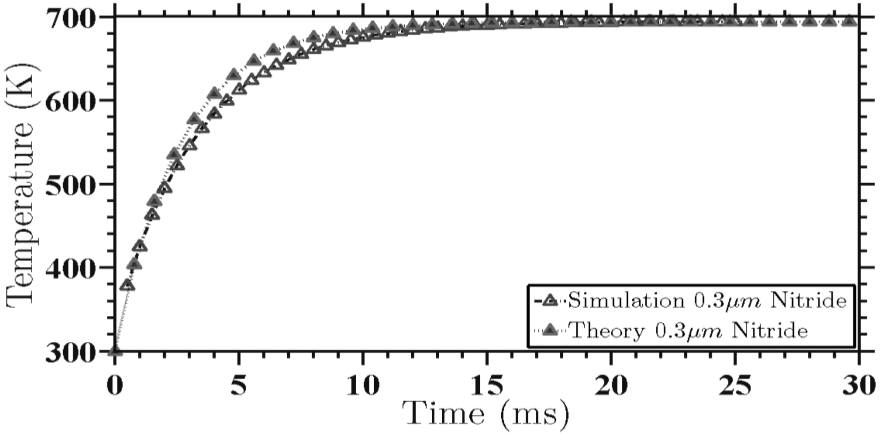
$$R_{Arm} = \frac{L_{Arm}}{K_{Arm}A_{Arm}} = \frac{L_{Arm}}{K_{Arm}T_{mem}W_{Arm}} (4)$$

$$R_{Cen} = \frac{L_{Nit}}{2K_{Cen}A_{Cen}} = \frac{L_{Nit}}{2K_{Cen}(T_{mem} + T_{top})L_h}$$

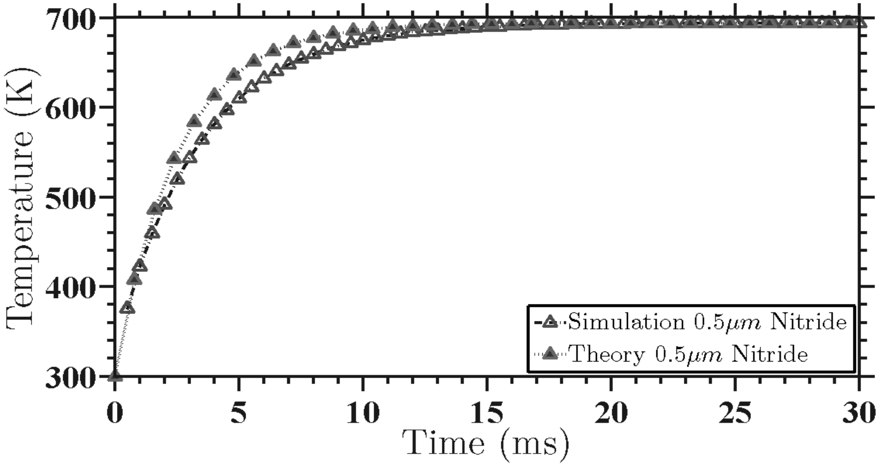
$$C_{tot} = 4 \times C_{Cen} = 4L_{nit}(T_{mem} + T_{top})L_h((\rho c_p)_{Cen})$$



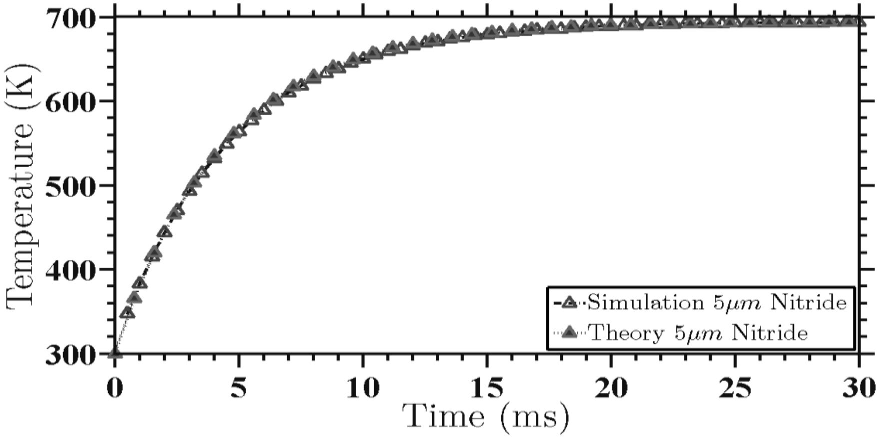
700
600
500
400
300
0
5
10
15
20
25
30
Temperature (K)
Time (ms)
Simulation No Nitride
Theory No Nitride



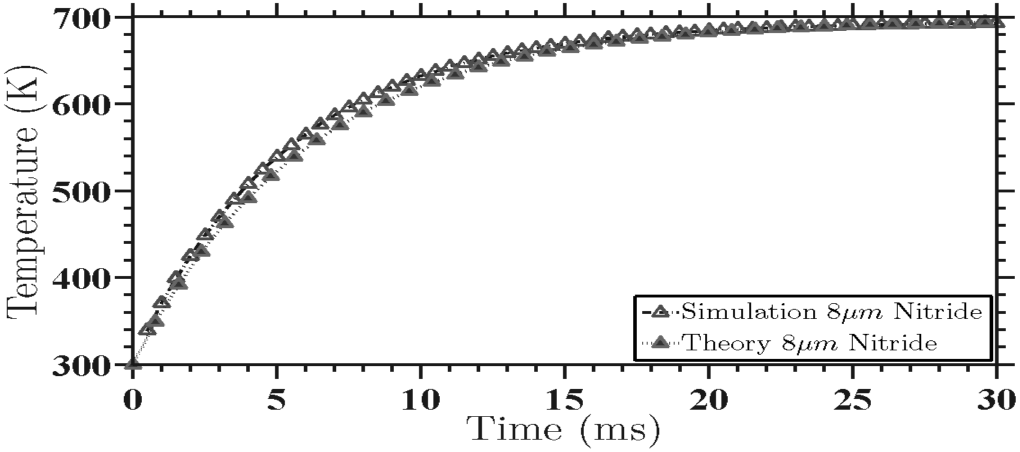
700
600
500
400
300
0
5
10
15
20
25
30
Temperature (K)
Time (ms)
Simulation 0.3μm Nitride
Theory 0.3μm Nitride



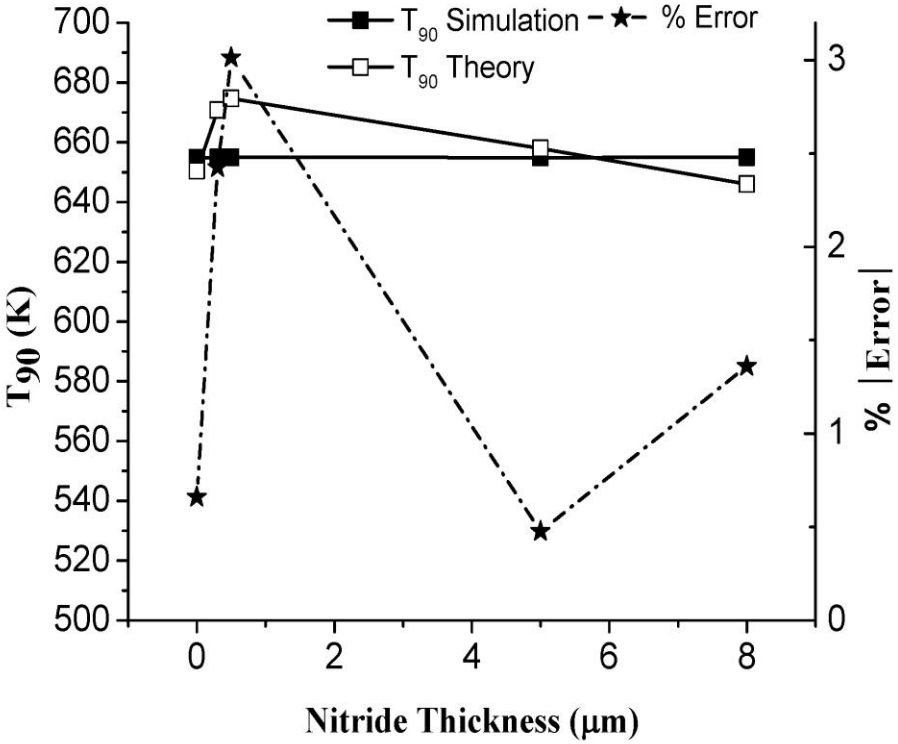
700
600
500
400
300
0
5
10
15
20
25
30
Temperature (K)
Time (ms)
Simulation 0.5μm Nitride
Theory 0.5μm Nitride

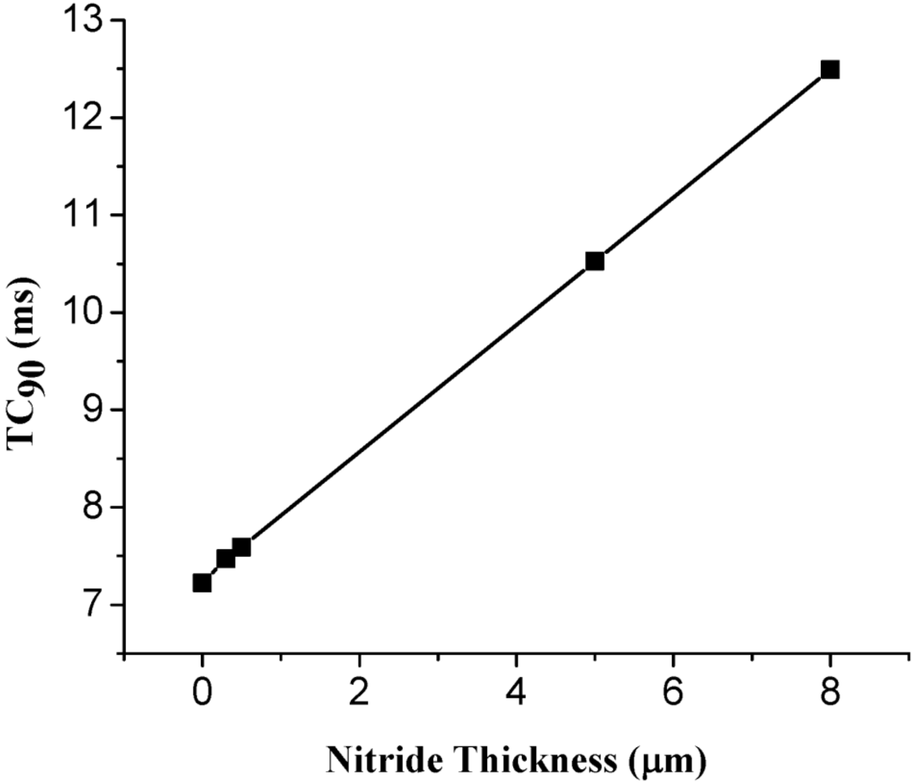


700
600
500
400
300
0
5
10
15
20
25
30
Temperature (K)
Time (ms)
Simulation 5μm Nitride
Theory 5μm Nitride



700
600
500
400
300
0
5
10
15
20
25
30
Temperature (K)
Time (ms)
Simulation 8μm Nitride
Theory 8μm Nitride


T90 Simulation
% Error
T90 Theory
T90 (K)
700
680
660
640
620
600
580
560
540
520
500
% |Error|
3
2
1
0
0
2
4
6
8
Nitride Thickness (μm)


TC90 (ms)
13
12
11
10
9
8
7
0
2
4
6
8
Nitride Thickness (μm)